BRE316R1/D

TMOS Power FET Design Ideas

MOTOROLA

MOTOROLA

TMOS Power FET Design Ideas

The circuits in this brochure represent the top 50 circuits selected from hundreds of circuits that were entered in the Motorola TMOS design contest. The entries were judged for originality and creativity as well as for opening new avenues of efficiency, simplicity, economy, uniqueness, functionality and performance. The entries were judged by a panel of engineers at Motorola and the winning entries were selected by a staff at Electronic Design News.

These circuits are published to give you an idea of some of the applications that power MOSFETs can serve and to stimulate your thoughts to design with the state-of-the-art power control devices — Motorola TMOS power FETs.

Congratulations to those that won and thanks to all those that participated in the contest.

TMOS is a trademark of Motorola Inc.

Issue B

TABLE OF CONTENTS

Circuit Techniques

Illumination

Miscellaneous

Motor Speed Control

Power Sources

RF Communications

Servo Amplifiers

TMOS Power MOSFET Selector Guides

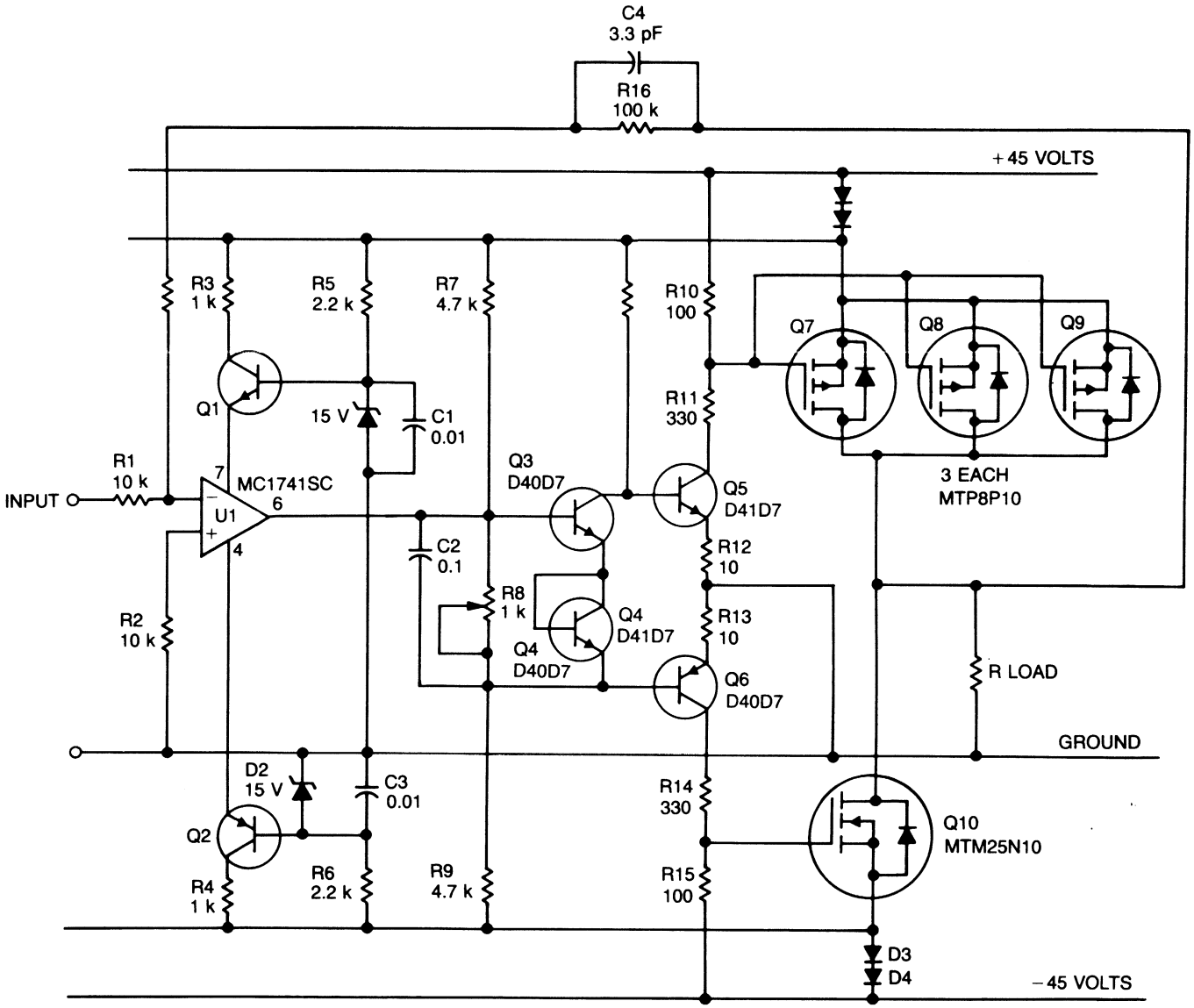
50 W Audio Power Amplifier

Jack D. Grimes, *San Jose, CA*

This audio amplifier design approach employs TMOS Power FETs operating in a complementary common source configuration. They are biased to cutoff and then turn ON very quickly when a signal is applied. The advantage of this approach is that the output stage is very stable from a thermal point of view.

Turn-on switching speed must be very fast in order to obtain very low harmonic and phase distortion. Bipolar output transistors cannot provide the desired results, but TMOS devices are much faster with better SOAs and can produce the desired results.

U1 is a high slew rate operational amplifier that drives Q3, Q4, Q5 and Q6 (operating Class AB) that provide level translation for the output stage consisting of Q7, Q8, Q9 and Q10. The positive temperature coefficient of the TMOS devices enables parallel operation of Q7, Q8 and Q9 and provides a higher power "complementary" device for Q10. These TMOS Power FETs must be driven from a low source impedance, $<100\Omega$, in order to actually obtain high turn-on speeds.



Class-D Power Amplifier

Aldo Cugnini, *Stamford, CT*

Requirements for a Class "D" power amplifier are much tighter than those for more conventional amplifiers. Output devices must be able to pass a substantial amount of current and have an extremely low ON resistance.

In this circuit, a 2-MHz clock is divided by eight in U1, providing a stable 250 kHz carrier. Q1 and Q2 buffer the clock and provide a low impedance drive for operational amplifier U4, which is a high gain amplifier and integrator. U4 accepts audio inputs and converts the 250 kHz square wave into a triangular wave. The summed audio and triangular wave signal is applied to the input of comparator U7 where it is compared with a dc reference to produce a pulse width modulated signal at the output of U7.

The differential outputs from U7 drive high speed opto-isolators U9 and U10, which isolate the input stage from the high voltage output stage. The two isolators drive upper and lower circuits that are identical except for their respective power sources. The lower section derives its power from regulator U12, whose input is 20 V above the −50 V supply (i.e., −30 V). The upper section gets its power from a high frequency power inverter consisting of U11, RS flip-flop U2, driver U3, pulse transformers T1 and T2, and diode D4.

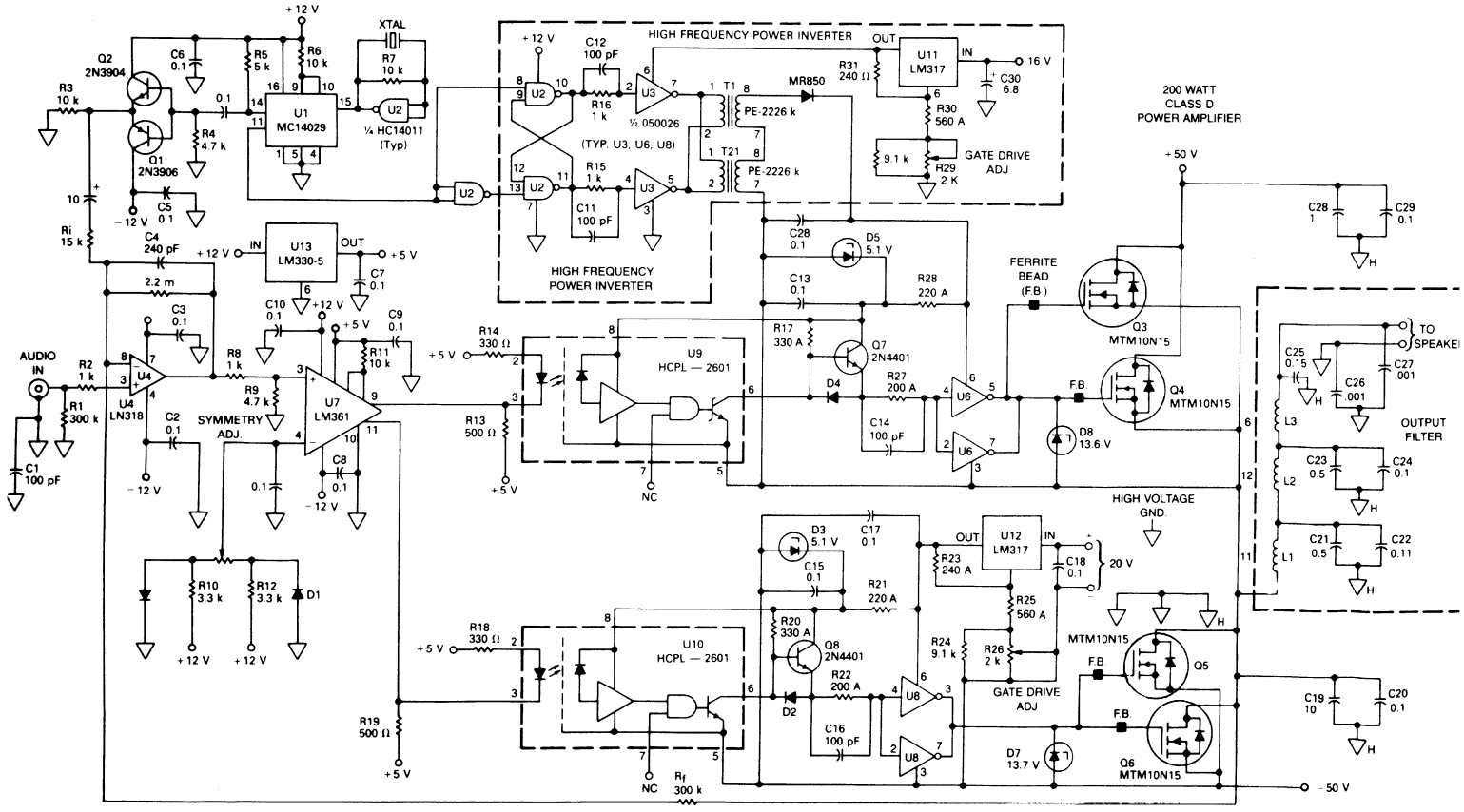
Pin 6 of U9 is connected to an active pull-up circuit and applied to clock driver U6, which is a high speed, high current source and sink. Outputs from U6 drive Q3 and Q4 TMOS devices, whose gates are protected by zener D8.

Q3 and Q4 require V_{GS} to be referenced to the output line, so a bootstrap supply is needed. This is the reason for the high frequency power inverter circuit.

Pin 6 of U10 also has an active pull-up circuit and its signal is applied to clock driver U8. Outputs from U8 drive Q5 and Q6 TMOS devices, whose gates are protected by zener D7.

The output devices switch between the +50 V and −50 V rails in a complementary fashion, driving the output filter that is a sixth-order Butterworth low pass type, which demodulates the audio and attenuates the carrier and high frequency components. Feedback is provided R_f; amplifier gain is R_f/R_i.

SPECIFICATIONS: 200 W continuous power into a 4Ω load; 20 to 20 kHz frequency response +0.5, −1.0 dB @ 200 W; THD, IMD <0.5% @ 200 W; 1.5 V RMS input for rated output; 69 dB S/N ratio, "A" weighting; 6.6 V/μsec slew rate.



Automotive Air Conditioner "Smart" Clutch

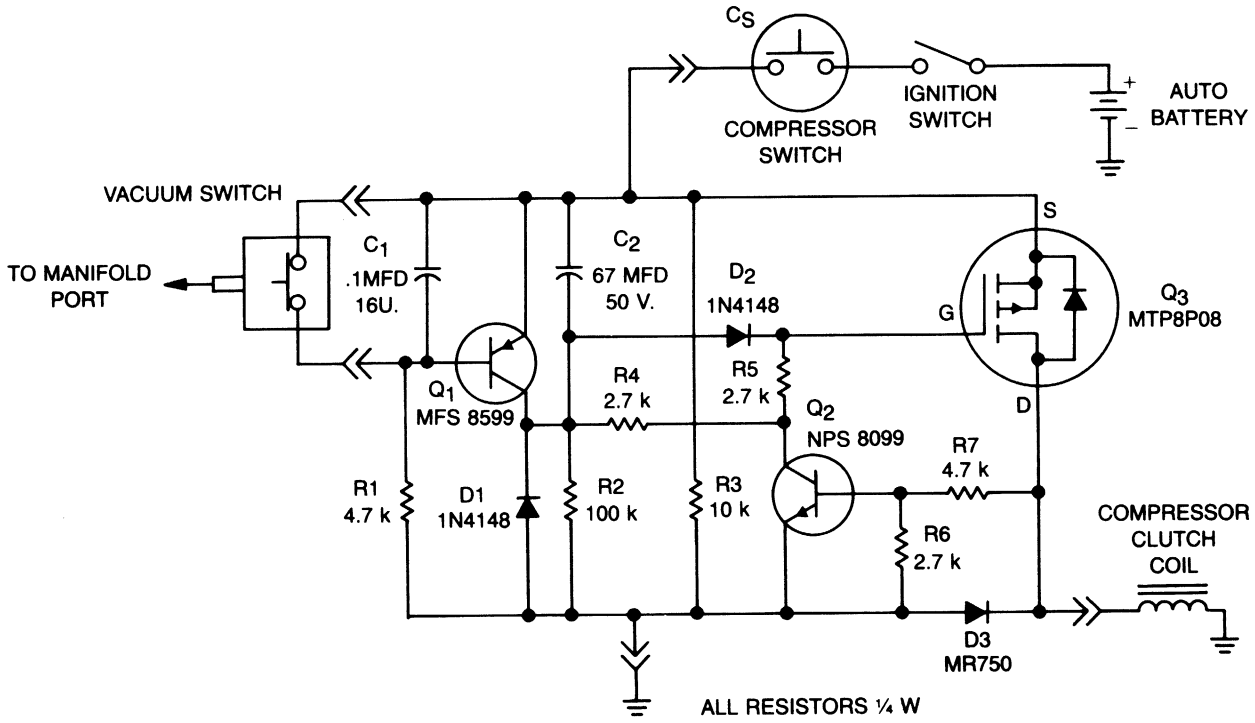
Stan Sitts, *Madison, WI*

Unnecessary auto engine loading, such as an air conditioner, can become a safety factor because it reduces acceleration and slows response time. For example, an automobile air conditioner requires 3 to 5 HP from the engine during normal operation.

The "Smart Clutch" solves the air conditioner loading problem by disabling the air conditioner compressor when additional engine power is required. It does so by monitoring the engine vacuum at the intake manifold. If the vacuum drops to 40% of its normal level, the compressor clutch is disabled, removing the air conditioner load from the engine. After the engine returns to a normal vacuum level, there is 6 sec delay, the compressor clutch is enabled and the air conditioner is activated. This allows 6 sec of extra power (about 500 ft at 60 MPH), which increases the safety margin when passing another vehicle. Loss of cooling is minimal because the air conditioner fan in not interrupted. When the engine is accelerated, manifold vacuum drops and vacuum switch, VS, opens at 40% of the normal manifold pressure. This causes Q1 to turn ON, discharging C2 and turning OFF Q3 via diode D2. When Q3 turns OFF, so does Q2. When the engine reaches its normal operating vacuum, VS closes and Q1 turns OFF, allowing C2 to charge for six seconds until Q3 turns ON again.

Another situation to be considered occurs when the engine is started with the air conditioner ON, which puts an additional load on the starter and battery. For this situation, the compressor switch, CS, and the ignition switch are closed, applying 12 V to the R2-C2 time constant. The C2 charging voltage appears at the gate of the MTP8P08 (Q3) via R4 and R5. Q3 starts to turn ON after six seconds, when its threshold voltage is exceeded. When Q3's drain voltage reaches 1.5 V, it turns ON Q2, which switches Q3 ON faster and applies power to the compressor clutch coil. During this time, the vacuum switch is closed because manifold pressure is high; thus, Q1 has no effect. During normal operation, as compressor switch CS cycles, the 6 sec delay is in effect and diode D1 allows rapid discharging of C2 via R3 and D1. Capacitor C1 helps keep vacuum switch VS contacts clean and reduces RFI susceptibility. Diode D3 is optional; it is a coil snubber for EMI reduction.

Vacuum switch requirements for 8-cylinder engine: mechanical contacts open at 4-in. vacuum and close at 6-in. vacuum. The sensor is similar to Fairchild PSF100A pressure sensor. Motorola MPX100 or MPX200 Series transducers with a ported package and an amplifier could replace VS and Q1.



Intermittent Windshield Wiper With Dynamic Braking

Vincent Salerno, *Hicksville, NY*

This circuit provides a delayed windshield wiper and dynamic braking of wiper blades when they reach the rest position. Dynamic braking prevents the blades from overshooting, which might cause them to stop at a point where they might interfere with the drivers vision.

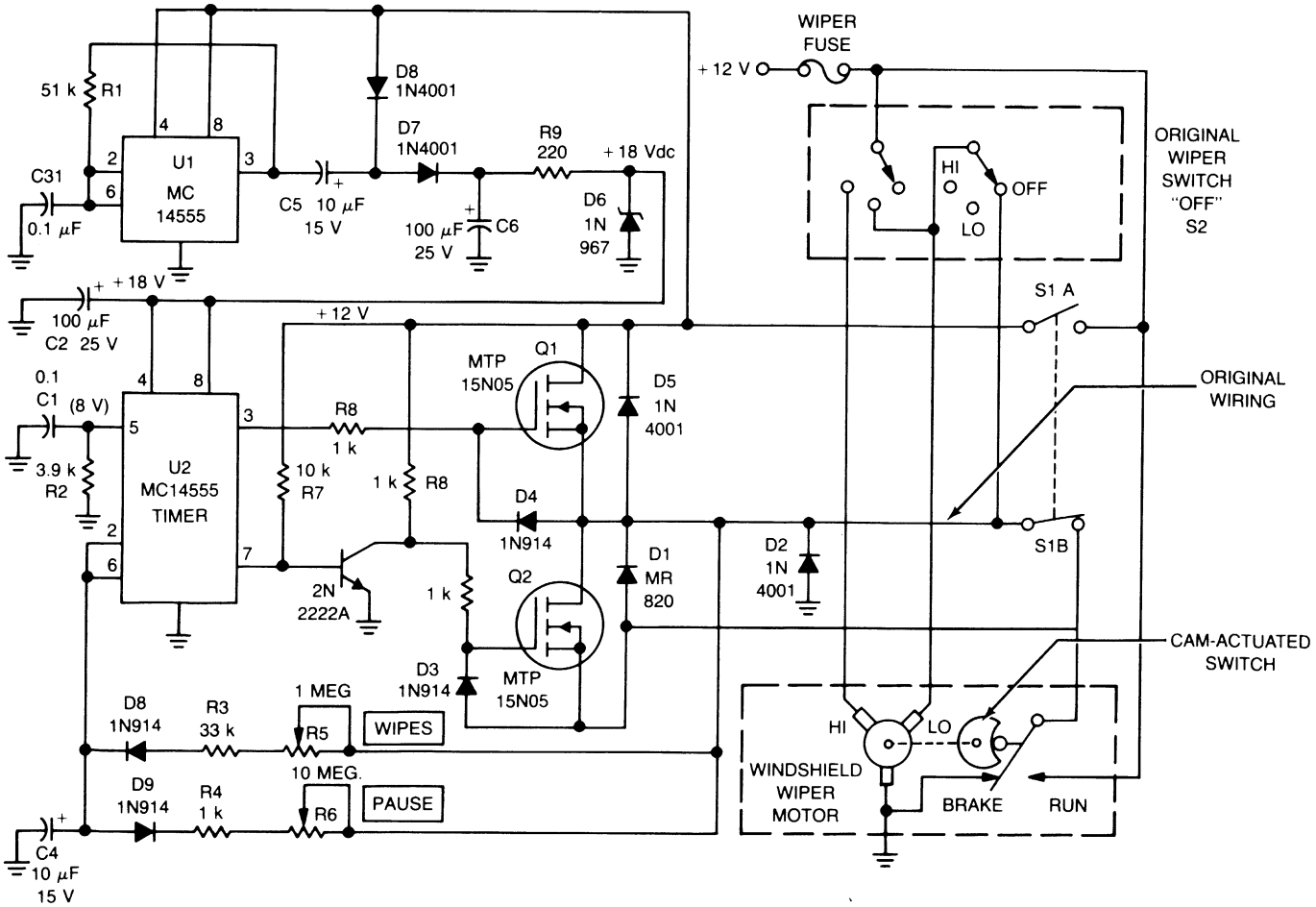
With the original wiper switch OFF, switch S1A turns ON the delay circuit and S1B disconnects the original automotive wiring. When S1 is turned OFF, the original wiring controls the system and the delay circuit is bypassed.

Turning S1 ON applies the +12 V battery to U1, which is a voltage doubler that produces +18 V. This higher voltage supply is necessary to insure reliable turn ON of Q1 by multivibrator U2. This arrangement provides about +18 V to the gate of Q1, whose source is +12 V minus the V_{DS} drop of Q1.

The voltage from the common point of the Q1-Q2 "totem pole" is applied to the wiper motor (via S1A and the original wiper switch). This moves the cam-actuated switch from the BRAKE (ground) position to the RUN (+12 V) position and back to the BRAKE position when the wiper blades return to the rest position. When C1 reaches +8 V, U2 fires, turning Q1 OFF and Q2 ON if the cam switch has reached the BRAKE position. This places a short circuit across the motor terminals, dynamically braking it. If the cam switch is still in the RUN position, the motor continues to be energized through D1, and Q2 is turned OFF. When the cam switch reaches the BRAKE position, Q2 turns ON because the gate is +12 V and the source is at ground. Again, the motor is shorted and dynamically braked.

Q1 remains ON for a time determined by the WIPES potentiometer that controls the number of wipes before pausing. The interval between wipes is controlled by the PAUSE control. When C1 drops below +4 V, U2 fires, turning Q1 ON and restarting the cycle.

Diodes around Q1 and Q2 provide protection against transients generated by the motor. D2 is a "free-wheeling" diode that prevents a large back EMF from being generated by the motor when the power is suddenly removed.



NiCad Battery Protection Circuit

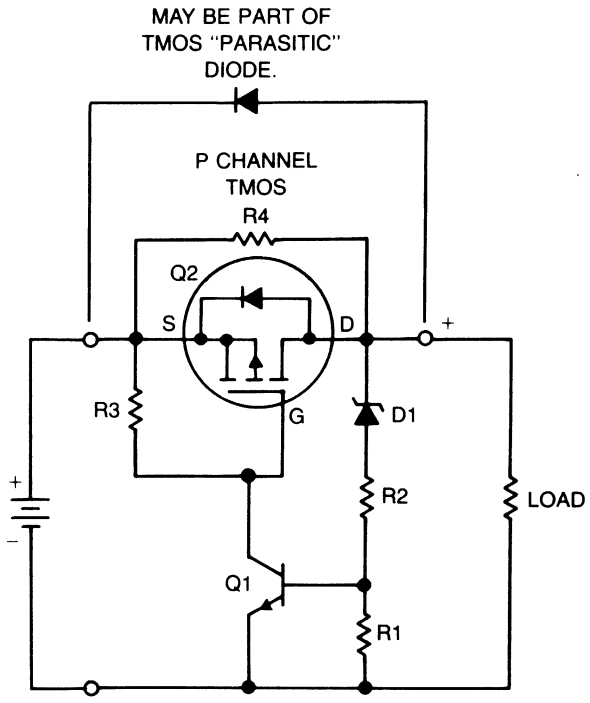
L. A. Turner, *Atlanta, GA*

If a NiCad battery is discharged to a point at which the lowest capacity cell becomes fully discharged and reverses polarity, that cell will usually short internally and become unusable. To prevent this type of damage, this circuit detects a drop of 1.25 V (one cell voltage) and turns the load OFF before cell reversal can occur.

This circuit takes advantage of the high input impedance and low series resistance of TMOS devices to keep the circuit power consumption so low that battery shelf life, or self-discharge time is not affected.

A low current zener or other voltage sensor (D1) and resistors R1 and R2 establish a reference level for transistor Q1. These resistors bias the zener to a few microamperes above its "knee". Therefore, if battery voltage falls more than 1.25 V, Q1 turns OFF, turning OFF Q2, and disconnecting the load. After the load is disconnected, if the battery returns to nominal voltage, the high value of resistor shunting Q2 provides enough output voltage to "reset" the voltage sensor and turn Q2 back ON. If desirable, a shunt diode, D2, or the parasitic diode of the TMOS device (if suitable) allows the battery to be charged from the load terminals.

The protection circuit presents a shunt current of only 10 mA at nominal battery voltage, which is low relative to the internal leakage of the batteries.



Back-Up Battery System with Low-Battery Protection Circuit

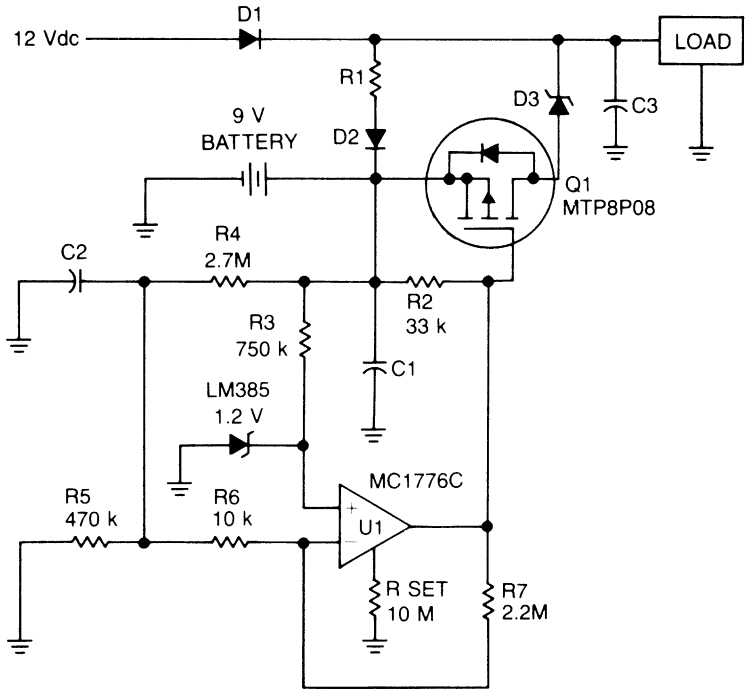
Djordje Boskov, *Lombard,IL*

A battery backup is commonly required when the operation of electronic circuits has to be extended during a power loss. The size of the backup battery is determined by the current consumption and the duration of the backup period. For an extended power loss there is a danger of over-discharging the battery, which can result in permanent battery damage.

To prevent battery damage, a low voltage detector and switch should be included in the design of the battery backup circuit. The detector circuit should consume extremely low current. The switch should exhibit a low voltage drop and be easy to control.

The circuit shown here is for use with a 9 V battery and very nearly satisfies the above criteria. It incorporates an MTP8P08 P-channel TMOS device (Q1) as a switch, an MC1776 (U1) programmable operational amplifier and a micropower voltage reference, LM385 (D4). U1 operates as a comparator with the advantage of a very low ISET.

In operation, R1 and D2 provide a trickle charge for the battery. Chosen for its low forward voltage drop, a Schottky diode (D3) prevents forward polarization of the diode incorporated in Q1. When the battery voltage is above approximately 8 V, the output of U1 is low and Q1 is turned ON. If the battery voltage falls below 8 V, the output of U1 goes high and turns OFF Q1.



Dynamic, Constant Current Load for Fuel Cell/Battery Testing

Christopher Ziolkowski, *Chicago, IL*

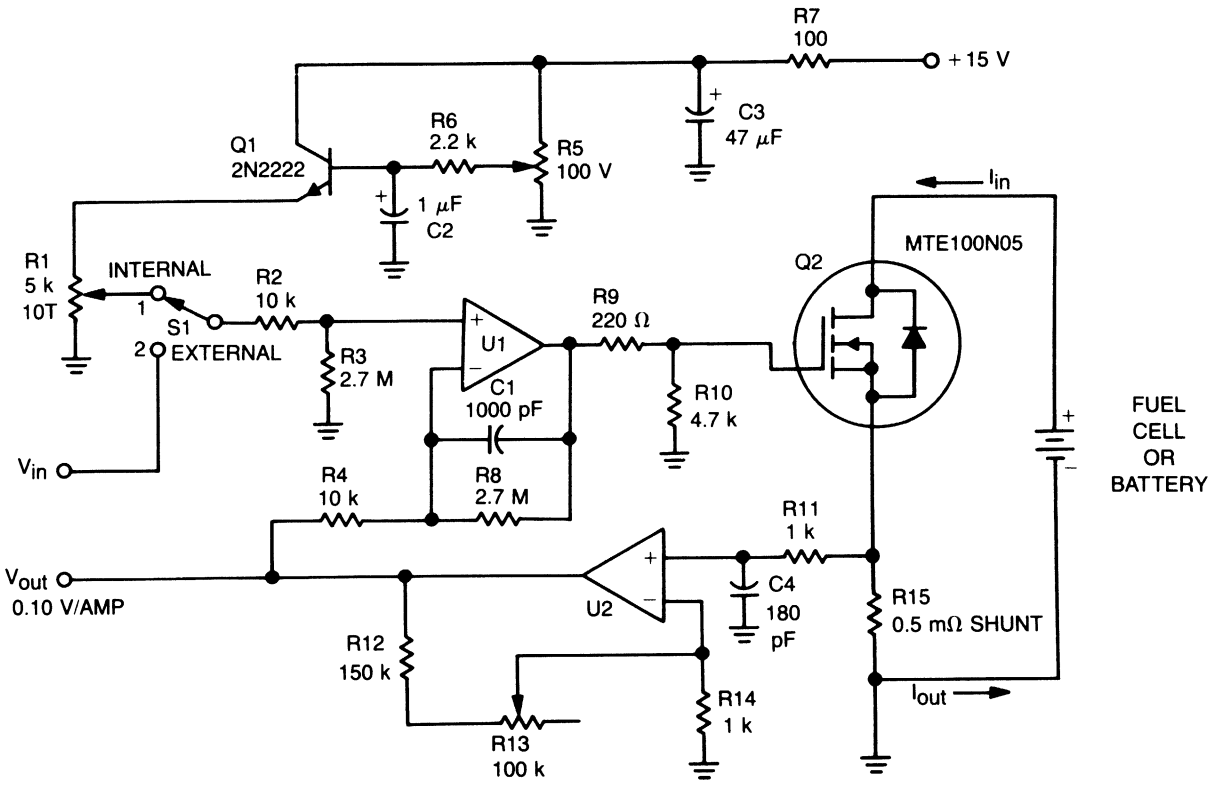
This circuit was designed for use in testing fuel cells, but it could also be used for testing batteries under a constant current load. It provides a dynamic, constant current load, eliminating the need to manually adjust the load to maintain a constant load.

The dynamic load can also be used for two other tests. First, the electrode capacitance can be measured under load by imposing an ac signal on top of the dc controlling the base load. Second, recovery time can be tested by loading the cell to a given current, then disconnecting the load, which allows the cell voltage to recover to its open-circuit value in a characteristic time. (The TMOS device can "disconnect" the load far faster than any mechanical switch). The dynamic load truly is dynamic because it provides a testing capability that is not possible with a passive load.

For fuel cell applications, the load must be able to absorb 20-40 A, and since a single cell develops only 0.5 to 1.0 V, bipolar power devices (such as a Darlington) are impractical. Therefore, this dynamic load was designed with a TMOS Power FET (Q2).

With switch S1 in position 1, emitter follower Q1 and R1 establish the current level for the load. In position 2, an external voltage can be applied to control the current level.

Operational amplifier U1 drives TMOS device Q1, which sets the load current seen by the fuel cell or battery. The voltage drop across R15, which is related to the load current, is then applied to U2, whose output fed back to U1. Thus, if the voltage across R15 should tend to change, feedback to the minus input of U1 causes that voltage (and the load current) to remain constant. Adjustment of R13 controls the volts/amp of feedback. The V_{OUT} point is used to monitor the system.



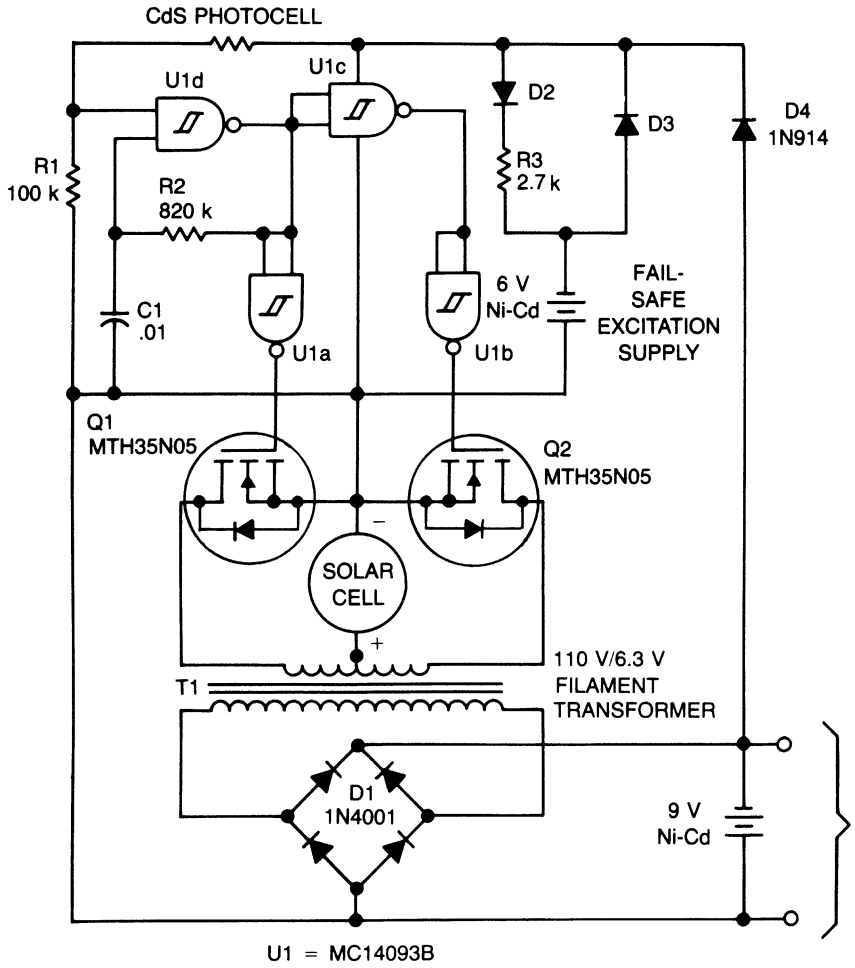
Battery Charger Operates On Single Solar Cell

Philip Smith, *Sandston, VA*

Operating from a single solar cell, the circuit shown charges a 9-V battery at about 30 mA per input ampere at 0.4 V. It can operate in a parallel battery configuration, that is, with a number of the same voltage cells in parallel. With the parallel cell system, changes in power requirements can be accommodated by merely adding or subtracting cells, whereas a series system must be completely redesigned to change power levels.

U1, a quad Schmitt trigger, operates as an astable multivibrator to drive push-pull TMOS devices Q1 and Q2. Power for U1 is derived from the 9-V battery via D4; power for Q1 and Q2 is supplied by the solar cell. The multivibrator frequency, determined by R2-C1, is set to 180 Hz for maximum efficiency from a 6.3 V filament transformer, T1. The secondary of the transformer is applied to a full wave bridge rectifier, D1, which is connected to the batteries being charged. The small NiCad battery is a fail-safe excitation supply to allow the system to recover if the 9-V battery becomes fully discharged.

A CdS photocell shuts off the oscillator in darkness to preserve the fail-safe battery during shipping and storage, or prolonged darkness.



Current-Driven Synchronous Rectifier

William R. Archer, *Fort Wayne, IN Grand Prize Winner*

A simple, two-terminal synchronous rectifier can be implemented with a TMOS Power FET, as shown in Figure 1. This configuration takes advantage of the Power FET's equivalent circuit, which can be considered as a conventional diode in parallel with a controllable resistor. When turned ON, the voltage across the Power FET is essentially a linear function of the current through it. This is true for both the conventional (drain-to-source) and reverse (source-to-drain) polarity. The reverse polarity is the normal forward conducting polarity of the synchronous rectifier.

A synchronous rectifier using a Power FET with a low $R_{DS(ON)}$ at the required current can provide better results than a conventional or Schottky rectifier. The MTM60N05 selected for this circuit has an $R_{DS(ON)}$ of less than 30 milliohms at 10 A.

Key to operation is toroidal current transformer, CT1, whose core is slipped over the wire connected to the source. CT1 has two secondary windings, one with three turns and the other with 25 turns. Therefore, a source current, IS, causes .04IS in the 25-turn secondary, which flows through diode D1 into the gate of Power FET Q1. This charges the input capacitance of Q1, turning it ON. Charging is terminated by saturation of CT1, which causes all windings to appear shorted. Therefore, transistor Q2 is solidly held OFF, D1 is reverse-biased, and the input capacitance of Q1 holds its charge. In this state, Q1 is fully enhanced and the resultant $R_{DS(ON)}$ effectively forces all the forward diode current through Q1, bypassing the internal parasitic diode. In this situation, Q1 acts as a high efficiency diode.

The saturated core of CT1 has a magnetizing current stored in it of a polarity that if unopposed would cause all the windings to reverse their original polarity. That is, the three-turn secondary would make the base of Q2 positive, turning it ON. This would rapidly discharge the input capacitance of Q1 and turn it OFF, allowing the synchronous rectifier to block current flow from "C" to "A." The magnetizing current of CT1 is overpowered by the forward current flowing in the one-turn primary. However, when the external load circuit attempts to reverse current flow, this magnetizing current becomes dominant, turning Q2 ON and Q1 OFF.

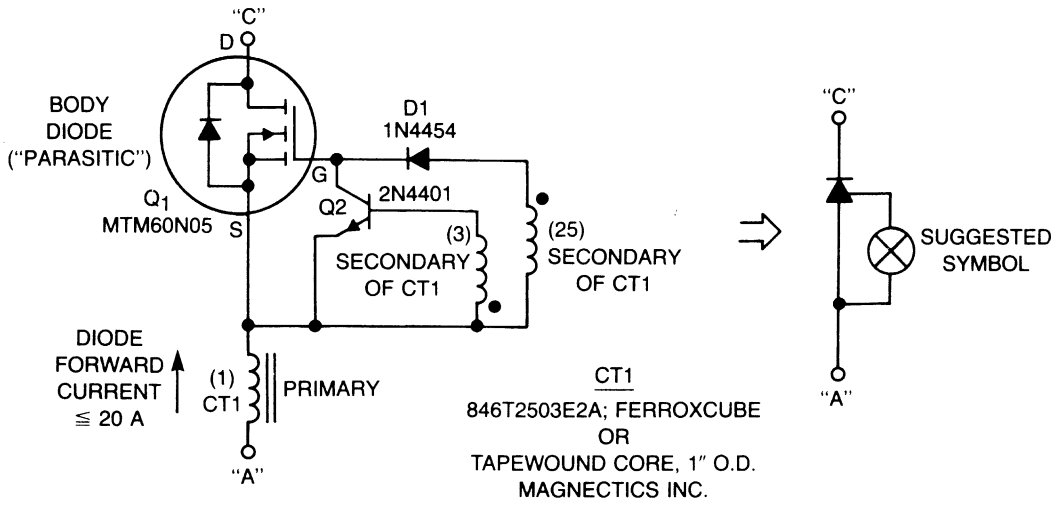
When the synchronous rectifier is blocking, CT1 is automatically reset. Also, Q2 base-emitter clamps the reset and guarantees that Q2 is conducting, which provides a low impedance from gate-to-source of Q1 during its critical high dv/dt recovery interval. This prevents false turn-ON even in "square wave" systems.

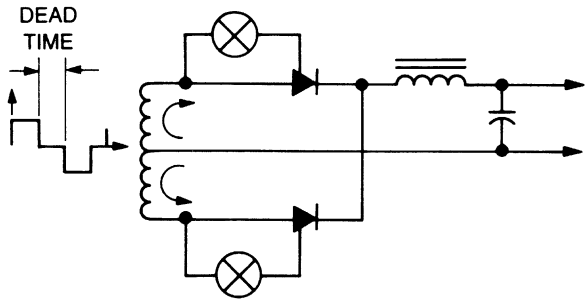
Turn-OFF time of the synchronous rectifier is controlled by Q1 and not the parasitic diode because the diode does not carry any current because the Power FET has effectively shorted it.

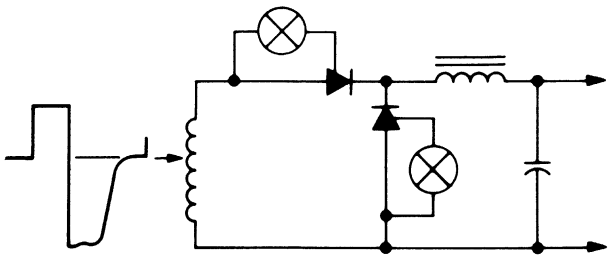
Proper turn-ON and turn-OFF of Q1 is accomplished by the actual load current without any external control or timing signals. Thus, the synchronous rectifier appears as a true two-terminal rectifier.

Figure 2 shows a full wave synchronous rectifier. Note that when this transformer is driven from a classic PWM converter with "dead time", the synchronous rectifier works perfectly. The inductor current divides equally between the two halves of the transformer and the two diodes, then it commutates when the next PWM stroke occurs. Note that during the "dead time" the secondary of the power transformer is essentially short circuited, thus eliminating the possibility of using auxiliary windings to drive a synchronous rectifier.

A forward converter for virtually any high frequency application is shown in Figure 3. There is no need for a special secondary winding to control the Power FETs and this would become especially difficult here anyway because of the lack of a common terminal. At very low current levels the Power FET may not be fully enhanced due to the lack of suitable drive, but the only consequence is that under this condition the load current flows in the parasitic body diode. At low current levels the benefit of the reduced Power FET voltage drop is not as important.


"C"
D
BODY
DIODE
("PARASITIC")
D1
1N4454
G
2N4401
Q2
Q1
MTM60N05
S
(3)
SECONDARY
OF CT1
(25)
SECONDARY
OF CT1
DIODE
FORWARD
CURRENT
≦ 20 A
(1)
CT1
PRIMARY
"A"
CT1
846T2503E2A; FERROXCUBE
OR
TAPEWOUND CORE, 1" O.D.
MAGNECTICS INC.
"C"
SUGGESTED
SYMBOL
"A"


DEAD
TIME



High Performance Isolated Gate Drive

Neil Rasmussen, *Burlington, MA* *Third Prize Winner*

Isolated Power FET gate drive circuits are necessary in many applications. One of the more widely used isolation techniques involves the opto-isolator, however these devices have a limited immunity to common mode swings (false triggering when the common mode dv/dt rating is exceeded). The best isolators have a common mode transient limit of only 1000 V/nsec. An off-line power supply or motor drive using a full of half bridge configuration can easily experience swings of 320 V in under 100 nsec with respect to the control circuits. This exceeds the limit of available isolators by a factor of three.

Another problem with opto-isolators is speed. Systems using opto-isolators require a power supply floating with each driven Power FET, and even the fastest opto-isolators are relatively slow compared to Power FETs.

Transformer isolation systems provide high speed, but suffer from severe problems in some applications. The maximum ON time is limited by core saturation and the minimum On time is limited by the magnetizing current that is needed to help turn OFF the Power FET. In addition, transformer duty cycle is usually limited to to 50%, maximum, for a simple system or 80% with a complex scheme. This fundamental limit occurs because the flux in the core must be reset by balancing volt-seconds after each Power FET ON period.

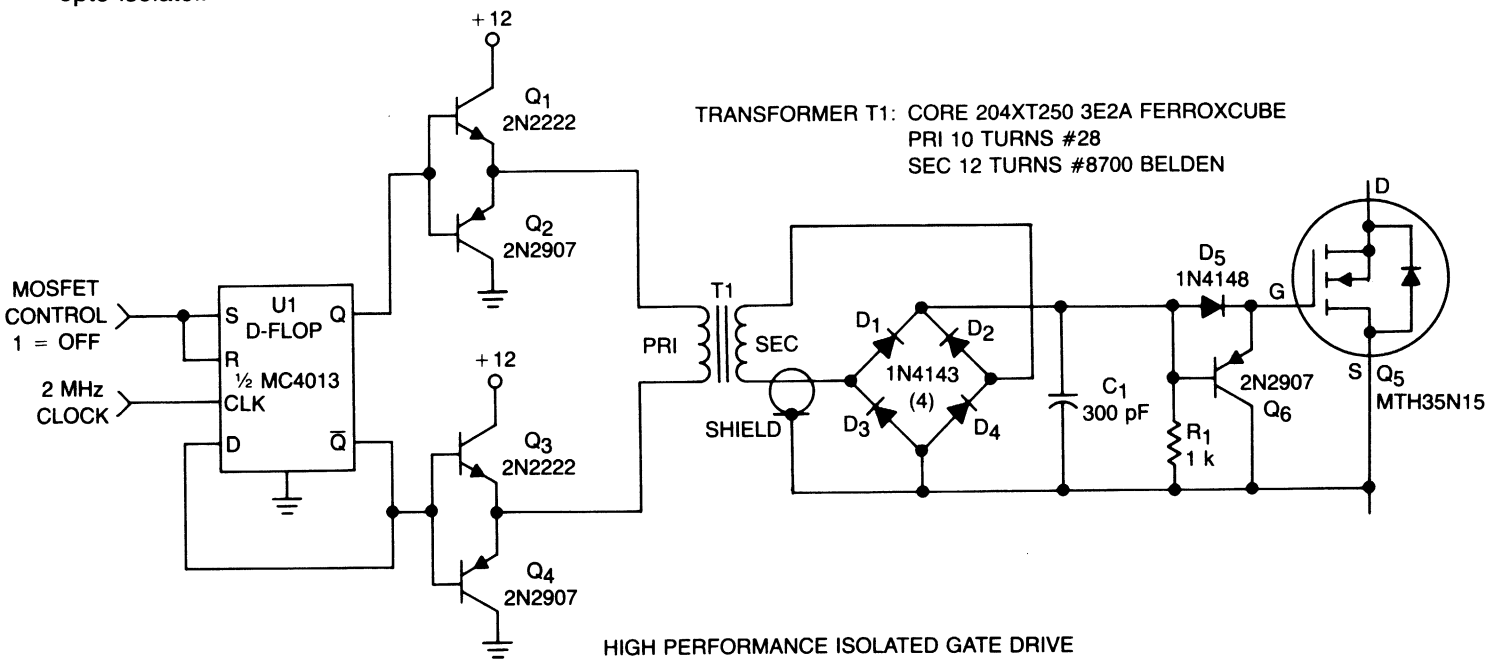
The "gated carrier" circuit shown here has the speed and common mode immunity advantages of the transformer isolation system combined with the unlimited flexibility of ON times and duty cycle offered by the opto-isolator.

In operation, a "D" flip-flop (U1) produces a 1 MHz carrier, which is gated by a control signal applied to the flip-flop. The Power FET ON voltage is supplied by rectifying the carrier; when the carrier is present, turn-ON bias is applied to Q5. To stop the carrier and turn Q5 OFF, the set and reset inputs are tied together and switched high, forcing both Q and $\overline{Q}$ to go high.

There is no limit to how long the carrier may appear at the transformer, and thus no ON time or duty cycle limitations. The transformer is much smaller than the kind used in a typical transformer drive because it handles 1 MHz instead of the normal 20 kHz. Because it is smaller and has fewer turns, this transformer has less leakage inductance and is less expensive than typical transformer drives.

Care must be taken in winding transformer T1 because any current flowing through the primary-to-secondary coupling capacitance is rectified by the diode bridge (D1-D4) and can cause false triggering of Q5. A common mode immunity of well over 10,000 V/μsec can be obtained by winding the secondary with miniature co-ax cable (Belden #8700). One end of the co-ax shield (not both) connects to the source lead of Q5.

Drive signals applied to T1 must also be carefully controlled. To prevent saturation, the carrier supplied to the transformer must have a duty cycle very close to 50%. This is guaranteed, independent of the clock frequency, by using the MC4013 flip-flop (U1) in its divide-by-two mode. This flip-flop alsq supplies complementary signals with very small overlap to T1, which guarantees a notch-free signal after the diode bridge.



HIGH PERFORMANCE ISOLATED GATE DRIVE

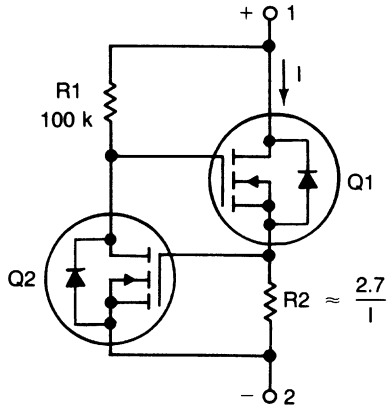
Constant Current, High Compliance Source/Sink

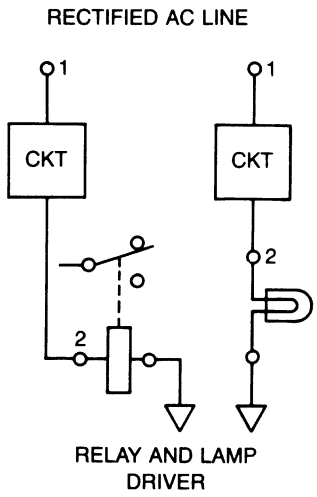
Richard Walter, *Parsippany, NJ*

The basic configuration for this constant current source/sink is shown in Figure 1. Initial positive biasing produces current flow in Q1 because its gate is forward biased. When sufficient current (I) flows, the voltage across R2 reaches the gate threshold voltage of Q2, which then conducts enough to force the Q1 gate to supply the current, I. R2 is approximately 2.7/I.

By using a a quad TMOS part, such as the MFQ990C, three sections can be paralleled to form Q1 and the fourth becomes Q2. With R2 = 135Ω, this circuit provides a compliance of 90 V at I ≈ 20 mA and 25°C ambient.

The circuit of Figure 2 shows applications as a lamp or relay driver. This technique provides a soft start for lamps, which increases their useful life. It also assures constant brightness over a wide supply voltage range. In addition, brightness control can be obtained by making R2 variable. For relays, it ensures reliable relay operation over a broad supply voltage range.





RELAY AND LAMP DRIVER

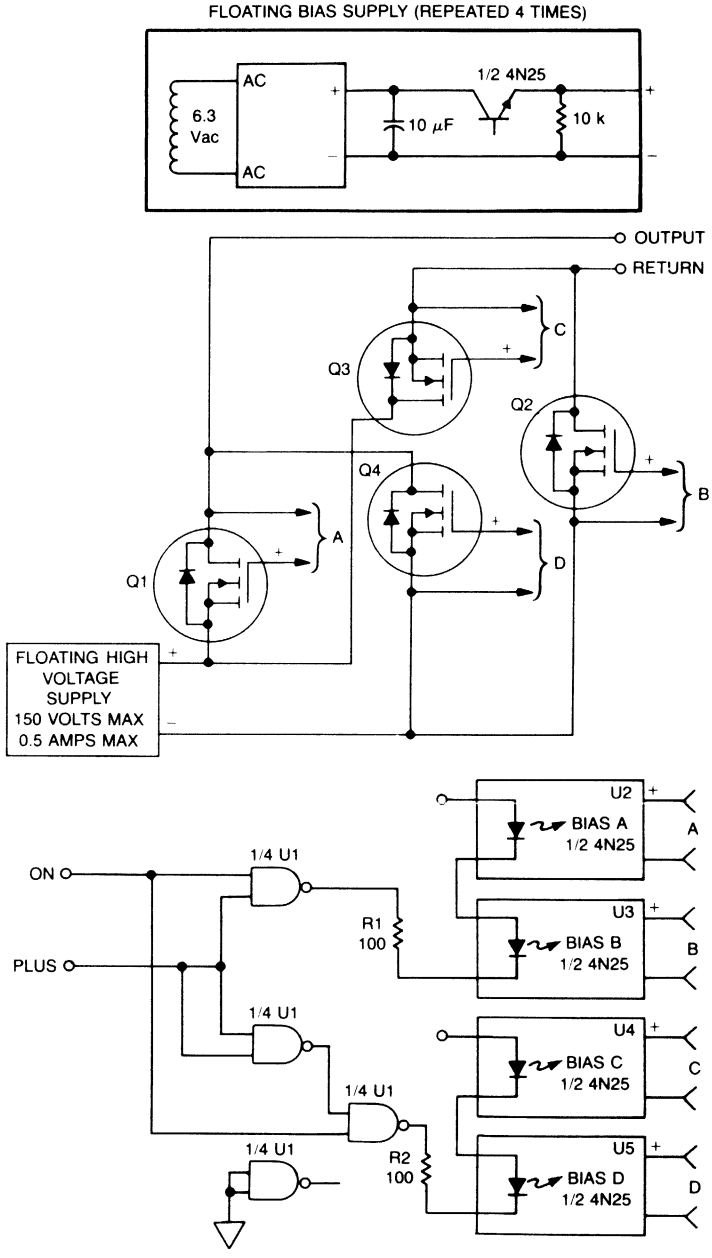
High Voltage Switching Circuit

Mike Willingham, *Mansfield, TX*

This high voltage switching circuit replaces a mechanical relay that is expensive and has a relatively short life. Although it occupies slightly more space than a relay, the advantage of reliability of the function is desirable. After one year there have been no failures in 15 installations. In contrast, every one of the original mechanical relay installations required service every three months. The cost-to-warranty reduction and increased customer satisfaction have repaid the conversion cost many times. Manufacturing costs have been lowered as well.

In operation, Q1 and Q2 are switched On in pairs, as are Q3 and Q4. Each of the four opto-isolators controls the output of a floating bias supply that rectifies 6.3 V ac and supplies a dc bias to turn ON one of these TMOS devices. A logic command applied to U1 causes the OUTPUT and RETURN of the high voltage power supply to change polarity.

If a logic command is given to turn ON the plus high voltage, opto-isolators U2 and U3 turn ON and opto-isolators U4 and U5 turn OFF. When this occurs, Q1 and Q2 are turned ON and Q3 and Q4 are turned OFF, the return side of the high voltage line is minus and the output is plus. If a polarity reversal is required, the logic input turns ON U4 and U5 and turns OFF U2 and U3, causing Q1 and Q2 to turn OFF and Q3 and Q4 to turn ON.



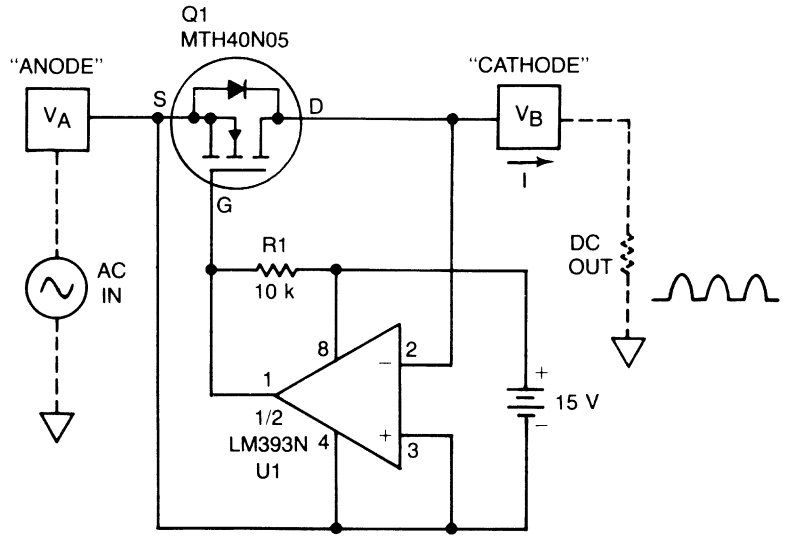
U1 — MC14011BCP
Q1, Q2, Q3, Q4 — MTP4N25

Low Forward Drop Rectifier Circuit

Bruce Rosenthal, *Sunnyvale, CA*

A TMOS Power FET (Q1) and an LM393 comparator (U1) can be used to provide a high efficiency rectifier circuit, as shown. When VA exceeds VB, U1's output goes high and Q1 conducts. Conversely, when VB exceeds VA, the comparator output goes low and Q1 does not conduct.

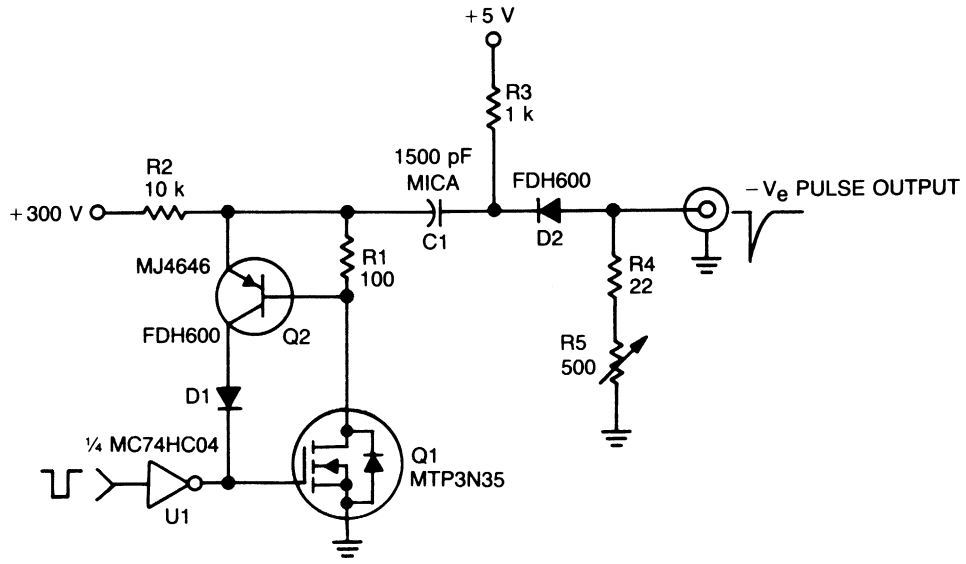
The forward drop is determined only by Q1's ON resistance and current I. The MTH40N05 has an ON resistance of 0.028 Ω; for I = 10 A, the forward drop is less than 0.3 V. Typically, the best Schottky diodes do not even begin conducting below a few hundred millivolts.



300 V Pulse Generator

Daniel Gray, *Calgary, Alberta, Canada*

In this TMOS pulser, a negative going pulse is applied to U1, a high speed CMOS buffer, which directly drives the gate of Q1, an MTP3N35. (If only a 100 V pulse is required, the MTP6N10 can be used.) The pulse output across R2 is differentiated by R3-C1 and appears as a negative-going spike at the output terminal.

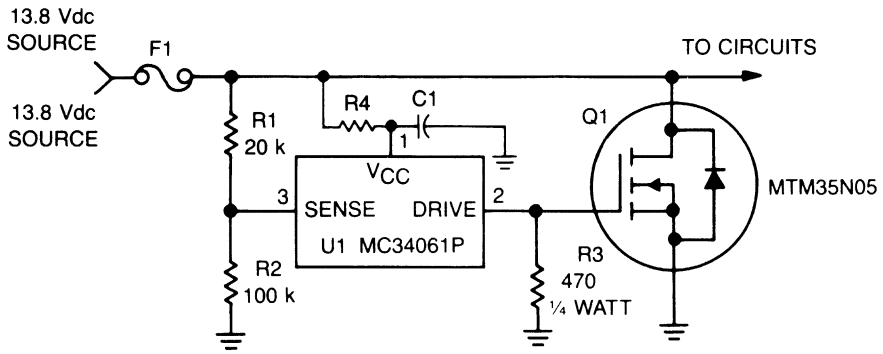


Fast Overvoltage Protection With No Latchup

Charles E. Browder, *Ft. Lauderdale, FL*

This circuit protects expensive portable equipment against all types of improper hookups and environmental hazards that could cause an over voltage condition. It operates very quickly and does not latchup, that is, it recovers when the overvoltage condition is removed. In contrast, SCR overvoltage circuits can latch and do not recover unless the power is removed.

Here, U1 senses an overvoltage condition when the drop across R1 exceeds 2.5 V. This causes U1 to apply a positive signal to the gate of Q1, turning it ON and shorting the line going to the external circuits. Fuse 1 opens if the transient condition lasts long enough to exceed the its i^2t rating. R4 and C1 may be required to suppress potential oscillations.

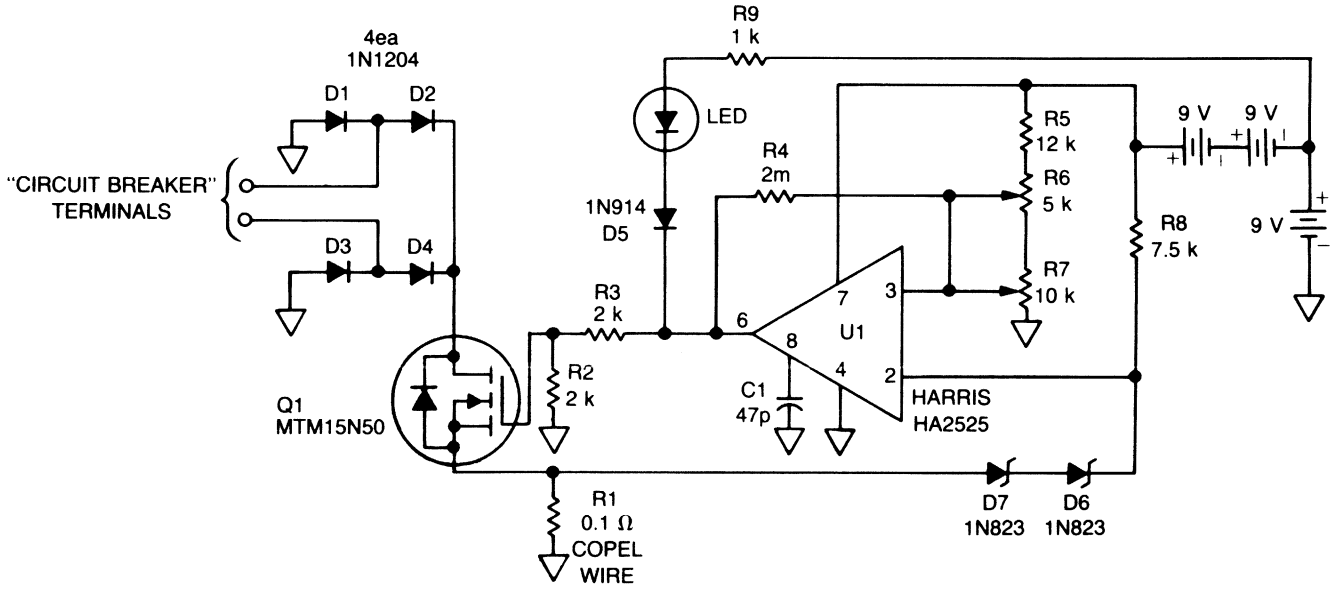


High Speed Electronic Circuit Breaker

D. Newton, *Culver City, CA*

This 115 VAC, electronic circuit breaker uses the low drive power, low ON resistance and fast turn OFF of the TMOS MTM15N50. The trip point is adjustable, LED fault indication is provided and battery power provides complete circuit isolation. These characteristics allow this circuit breaker to be inserted into a prototype power conditioning system during initial turn-ON and debugging. Circuit response time is close to the limits of the Power FET itself, which is adequate for many bipolar protection tasks.

The two "circuit breaker" terminals are across one leg of a full wave diode bridge consisting of D1-D4. Normally, Q1 is turned ON so that the circuit breaker looks like a very low resistance. One input to comparator U1 is a fraction of the internal battery voltage and the other input is the drop across zeners D6 and D7 and the voltage drop across R1. If excessive current is drawn, the voltage drop across R1 increases beyond the comparator threshold (determined by the setting of R6), U1 output goes low, Q1 turns OFF, and the circuit breaker "opens." When this occurs, the LED fault indicator is illuminated.



Line Driver Provides Full Rail Excursions

Stan Harrison, *Parker, CO*

A relatively simple logic signal line driver can be configured using complementary TMOS pairs to achieve full excursions to + and - supply rails.

The logic input is applied to opto-isolators U1 and U2. Dc balance is adjusted by potentiometer R2. The emitter followers drive the gates of Q1 and Q2, the complementary TMOS pairs. With a ±12 V supply, the swing at the common source output point is about 12 V peak-to-peak.

By adding a ±18 V boost circuit, as shown, the output swing can approach the rail swing. This circuit applies the output to transformer T1, which is rectified by diode bridge D3, regulated by U3 and U4, and then applied to the collectors of U1 and U2. Diodes D1 and D2 are forward-biased when 12 V supplies are used, but they are back-biased when the ,18 V boost is used.

Since any TMOS complementary pair may be used, a method for calculating the load is given by:

Load voltage = .714 X 12 V = 8.6 V RMS

From the FET derating curves, determine the maximum operating current. For the MTP8N10 @ 25°C, use 8 A.

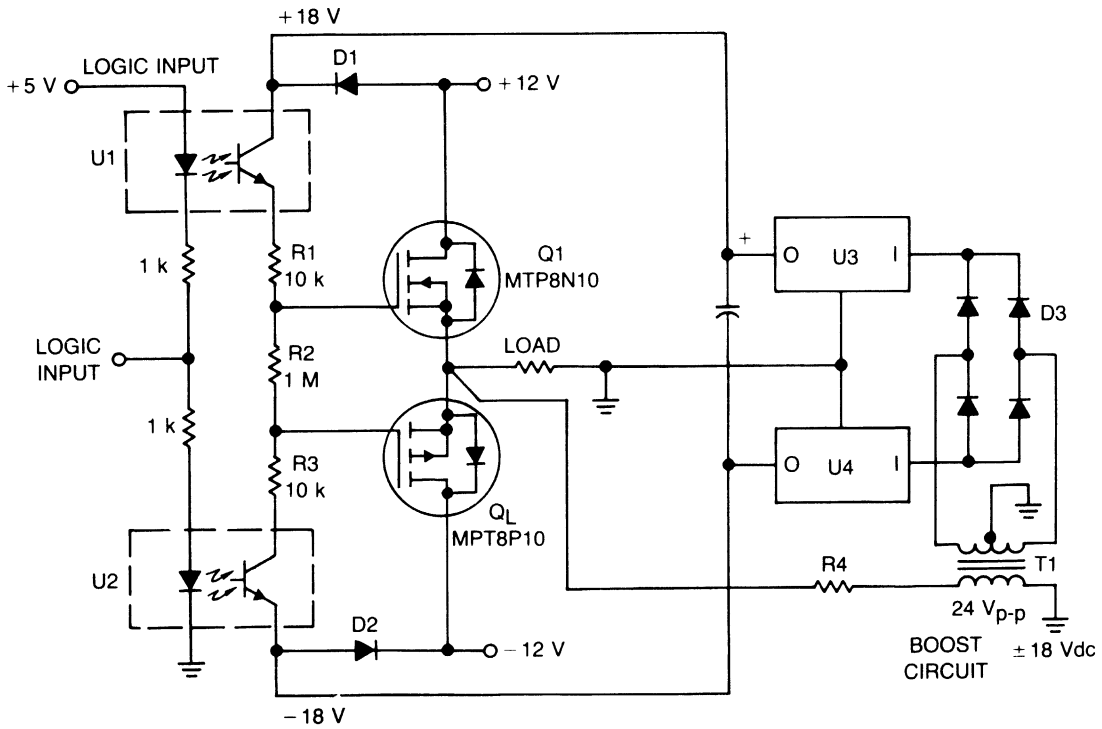
8 A X 0.5Ω = 4 V drop

8.6 − 4 V drop = 4.6 V RMS across R_{LOAD} @ 8 A

V = IR

4.6 = 8R

R = 0.575Ω, minimum load impedance or resistance

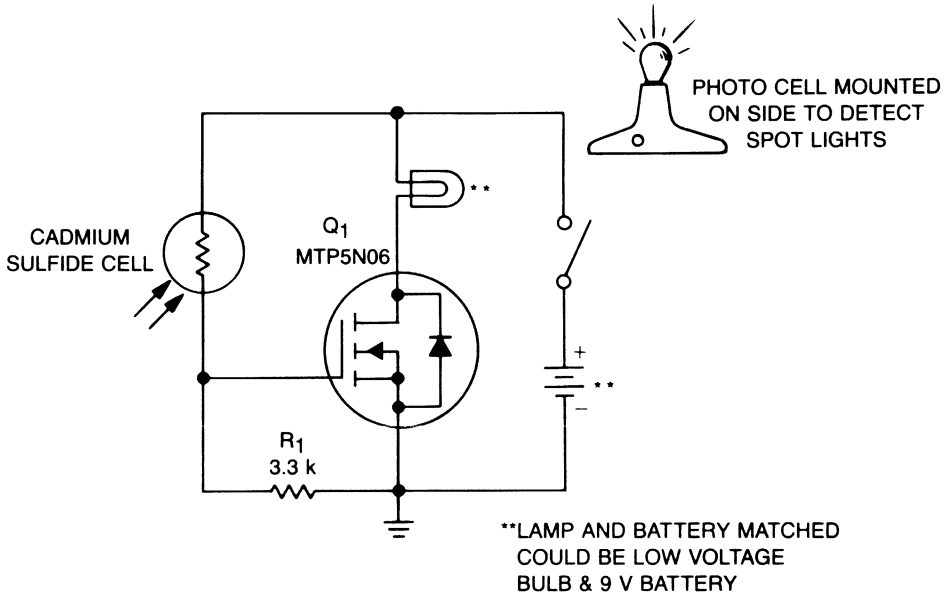


Light-Controlled Lamp Switch

Dennis Baldridge, *Bourbonnais, IL*

Our school drama department needed lamps that automatically went ON and OFF when spot lights did the same. Lamp switching had to be wireless, durable, dependable, simple and low cost.

With stage and spot lights OFF, very little light falls on the CdS photocell, so its internal resistance is several megohms and R1 keeps the gate of Q1 at nearly zero volts, which keeps it OFF. When a spot or stage light hits the photocell, its resistance drops to several hundred ohms, raising Q1's gate voltage, which turns it ON and applies power to the lamp.

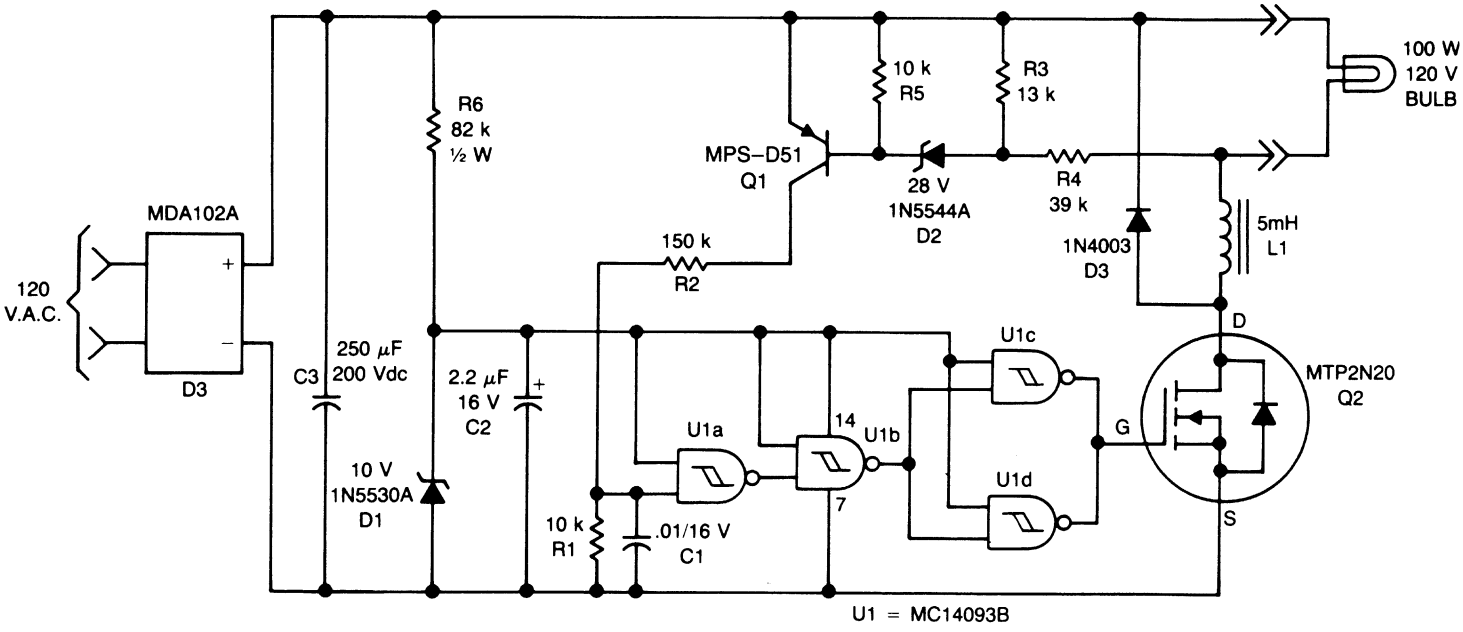


Machine Vision Illumination Stabilizer

Scott Juds, *Everett, WA*

Variation of machine vision system illumination with line voltage is one of the more significant problems to contend with in the industrial environment. Dropouts from large machines starting or just general variation throughout the day can affect illumination and detection reliability. This switching regulator circuit solves this illumination stabilization problem.

The combination of Q1, Q2 and U1 form a hysteresis oscillator to stabilize lamp illumination. In operation, full wave bridge D3 operates directly from the ac line to supply unregulated dc to the lamp and also to the 10-V zener that provides power to the quad CMOS Schmitt trigger, U1. When the lamp supply exceeds 115 V, Q1 is turned ON, charging C1 through R2 to raise the input to U1a past the positive-going logic threshold. This drops the output voltage at U1c and U1d, which drives the gate of Q2, turning it OFF. Current then decays through the lamp, L1 and D3 until the lamp voltage falls below 115 V, at which time Q1 turns OFF and the cycle repeats.



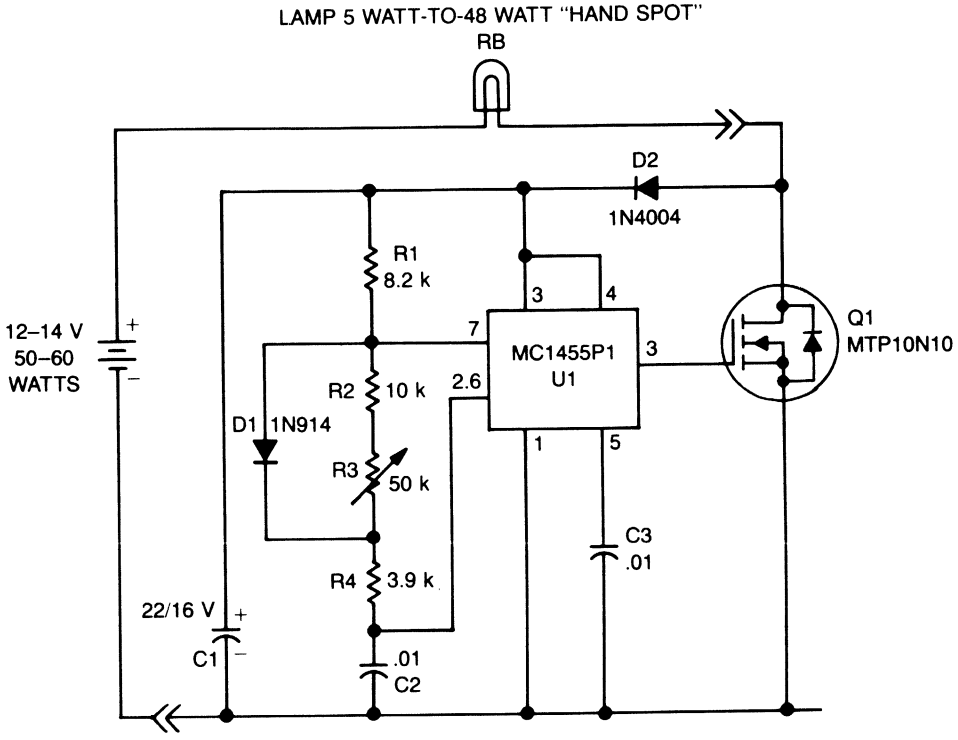
Illumination

DC Lamp Dimmer

Mark Molnar, *Bellville, OH*

A low power, low cost dc lamp dimmer for a two-wire portable "flashlights" can be realized with little or no heatsinking. In addition, a single potentiometer, R3 adjusts lamp brightness.

Battery power is stored in C1 for U1, which is a free-running multivibrator whose frequency is determined by R1, R2, R3, R4 and C2. U1 drives the gate of Q1, turning it and the lamp ON and OFF at a rate proportional to the multivibrator duty cycle.



Lamp Life Extender

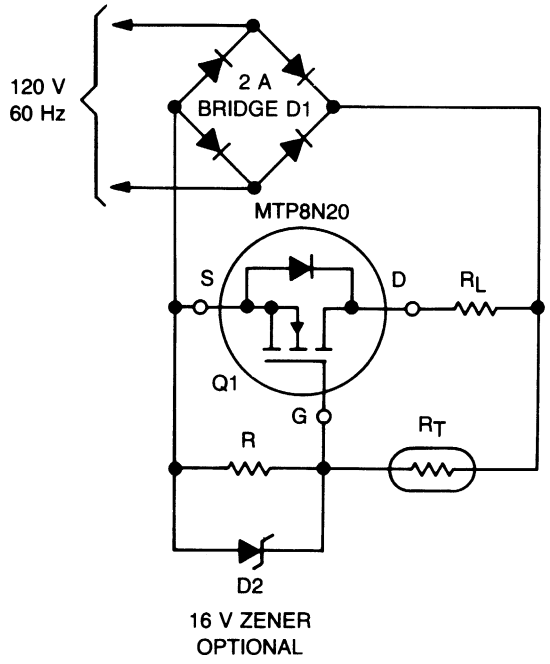
B. E. Anderson, *Rockville, MD*

Lamp life can be extended by improving the conditions under which its filament is operated. This includes eliminating the inrush overcurrent surge and reducing the mechanical stress (vibration) on the filament caused by an alternating current source.

The circuit shown controls the inrush current to the lamp without the 10 to 15 times rated current surge that normally occurs when power is applied to a "cold" lamp. It does so by adjusting the inrush current over time to the inverse of the value normally experienced.

RL is a standard tungsten lamp in the range of 15 to 250 W, R is 10 KΩ and RT is a negative temperature coefficient resistance that is initially 1.65 MΩ and decreases, by self-heating, to 150 KΩ in approximately 0.5 sec. Use of the TMOS device allows high ohmic values for R and R_T, keeping drive power at a negligible level.

This circuit has a number of advantages: very low power dissipation, long life and low cost components, no significant effect on lamp ratings, negligible effect on efficiency, negligible RFI and can be used in hazardous environments.



Safety Shutdown Monitor

Buddy J. Cook, *Tigard, OR*

Many industrial systems contain a safety shutdown circuit that takes control of equipment to prevent a safety hazard. The circuit shown here monitors such a safety shutdown circuit to ensure that it will operate properly, if necessary.

This circuit operates with several different loads and source voltages, either ac or dc supply; it also provides isolation and load protection if a circuit malfunction occurs.

The monitor is placed across across load switch S1, which turns on the power to load L1. Fuse F1 is selected to open before a failure could energize the load, because any failure in the monitor could turn on the load.

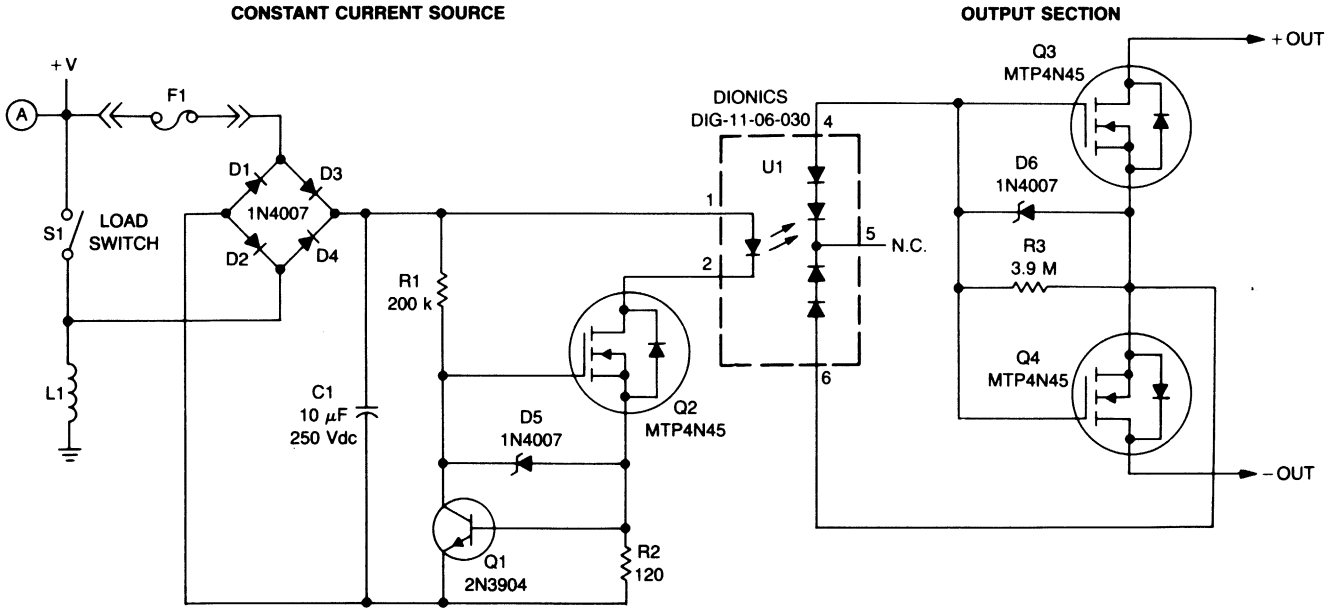
In operation, a TMOS-controlled current source, consisting of Q1, Q2, R1, R2 and D5, supplies a constant trickle current through L1. S1 is normally open, so no power is applied to the load. An external positive voltage is applied at point A, causing current flow through D3, U1, Q2, R2, D2 and the load. As the supply voltage begins to rise, Q2's gate rises at the same rate. When the gate-to-source voltage reaches the gate threshold, Q2 begins to conduct and the drain-to-source current begins to increase. Transistor Q1 conducts when the drop across R2 reaches 0.6 V, forcing the gate of Q2 more negative, which regulates its gate-to-source voltage and provides a constant current. This constant current source provides a fixed current in the opto-isolator (U1), so a constant open circuit voltage is presented to the output section.

The open circuit voltage output of U1 is sufficient to drive the gates of Q3 and Q4 past their respective turn-on thresholds. A single Power MOSFET can switch a dc voltage, however two such devices are required for ac.

The parasitic diodes are used to an advantage when switching ac. When a positive voltage is applied to the drain of Q3, its parasitic diode is back-biased. However, U1 produces a voltage that is positive relative to the source, so Q3 turns ON. Q4 is tied to Q3, so the current through Q3 must flow into the source of Q4. Therefore, Q4's parasitic diode is forward-biased, completing the circuit loop. When the polarity is reversed, the parasitic diodes are again forward-biased.

Zener diodes D5 and D6 protect the TMOS FETs from transients that could cause gate-to-source damage. R3 improves turn-off time by providing a lower gate resistance discharge path.

Two conditions cause the circuit to indicate a break in monitor current. One is when the current path is interrupted or broken, the second is when S1 is closed, shunting the current source. When the control system operating the switch determines a safety shutdown must occur, it toggles the switch (the switch is actually a redundant series/parallel combination). Since the control system was in an alarm state to turn on the switch, the monitor indication is meaningless. However, if monitor current is lost and the system does not call for a shutdown, an alarm is sounded.



Proportional Temperature Controller

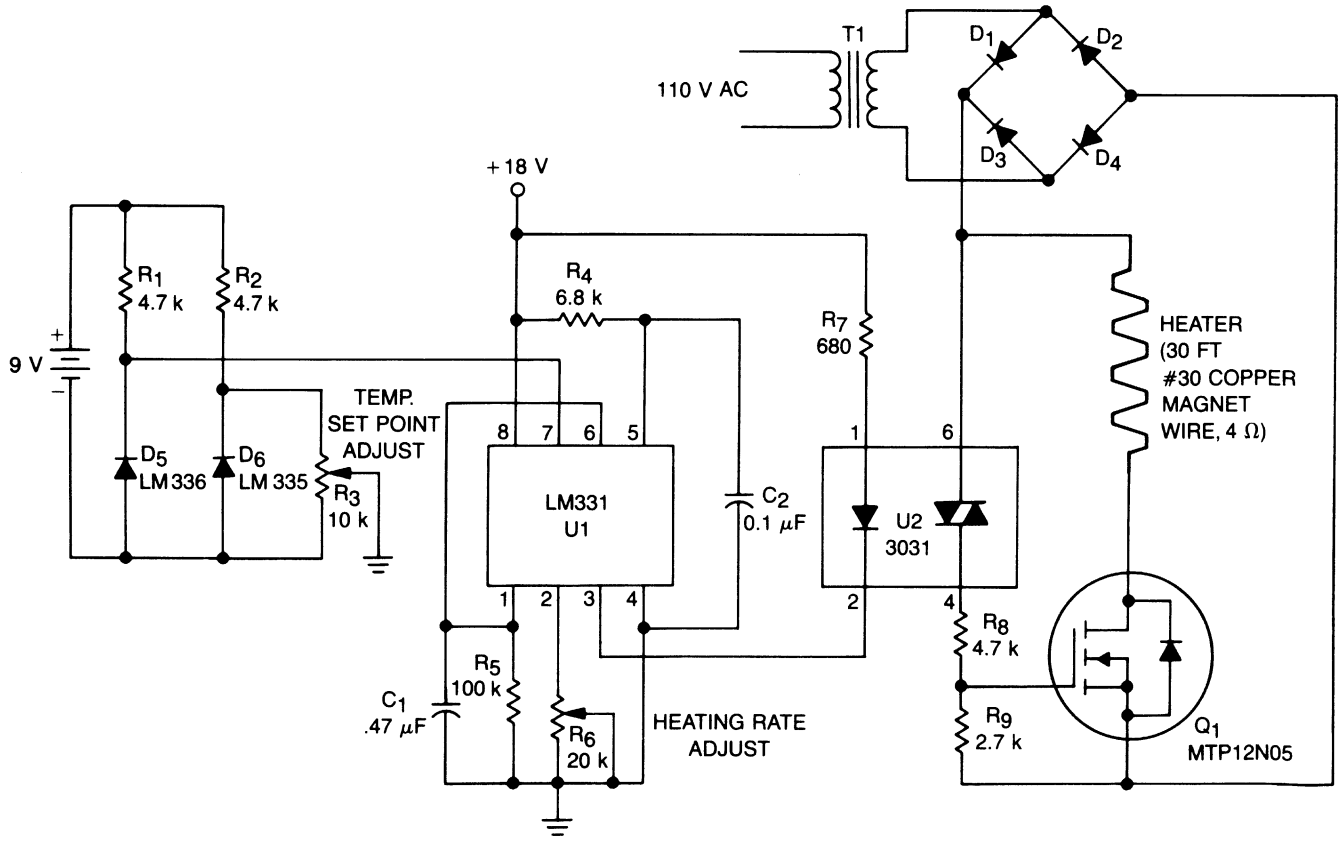
Douglas Jewett, *Ann Arbor, MI* *Third Prize Winner*

This temperature controller operates as a "pulse snatching" device, which allows it to run at its own speed and turn ON at the zero crossing of the line frequency. Zero crossing turn-ON reduces the generation of line noise transients.

In this circuit, a TMOS Power FET, Q1, is used to turn ON a chemical reactor's heater, which consists of 20 ft of #30 magnet wire (4Ω) wound tightly on the tapered end of a glass centrifuge tube. To improve heat transfer, D6, an LM335 temperature sensor, is cemented directly to the coil with silver epoxy. By doing this instead of the heating block or oil bath normally used, both heating and subsequent cooling of the reactor are very fast, and limited mostly by the time constant of the sensor itself.

Temperature sensor D6 provides a dc voltage proportional to temperature that is applied to voltage-to-frequency converter U1.

Output from U1 is a pulse train proportional to temperature offset that is applied to the input of the zero crossing triac opto-isolator U2. The anode supply for the triac is a 28 V peak-to-peak, full wave-rectified sine wave. The opto-isolator ORs the pulse train from U1 with the zero crossing of U2's anode supply, supplying a gate turn ON signal for Q1. Therefore, TMOS Power FET Q1 can only turn the heater ON at the zero crossing of the applied sine wave. Maximum temperature is limited by the sensor and the insulation of the wire, which is 130°C for the components shown.



120 kHz, 500 W Induction Heater

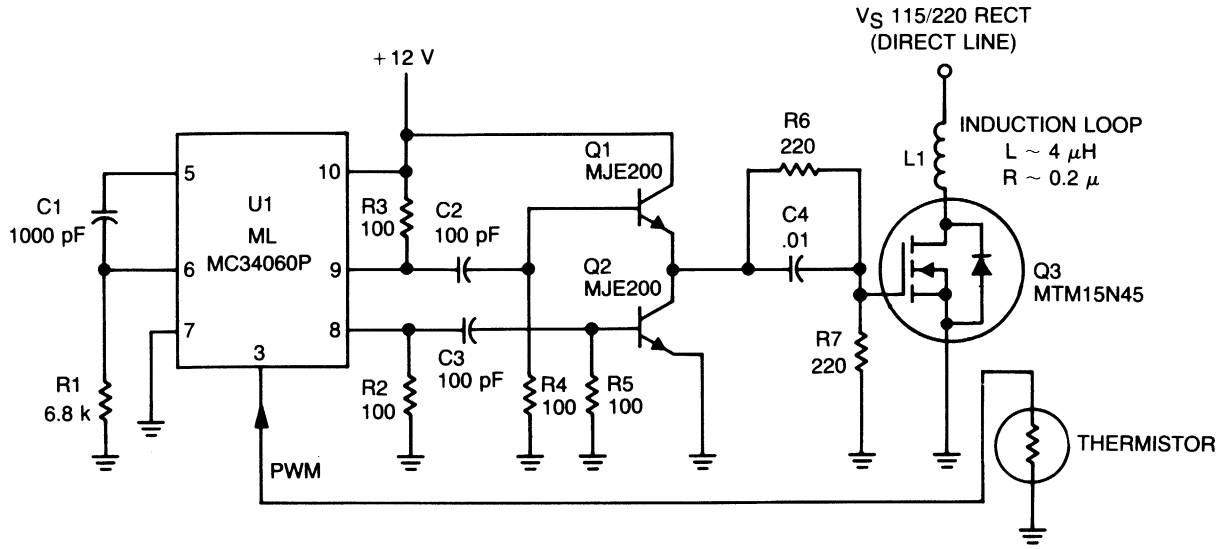
Ron Doctors, *Santa Barbara, CA*

An induction heater for flash heating of conducting solutions using TMOS requires fewer parts and operates at higher speeds than an equivalent bipolar version. Using TMOS also provides the option to increase the output rate without changing the design and allows a modular power concept. In addition, the integral TMOS diode saves an external diode (which is essential because of the possibility of an unloaded induction loop with very high induced flyback voltage).

Variable width pulses with fast rise times are provided by U1, an MC34060 operating at 120 kHz, the optimum frequency for heating aluminum alloy containers. The pulse width is modulated by sensing the temperature of the target with a thermistor, using its negative temperature coefficient to change pulse duration. The MC34060 produces output pulses that are ac-coupled to push-pull MJE200 transistors (Q1 and Q2). This provides the current needed to ensure fast switching of the MTM15N45 TMOS Power FET (Q3).

Estimated efficiency is 80%, based on switching losses and an R_{ON} of 0.4Ω (max). The MTM15N45, with maximum ratings of 15 A and 450 V, was chosen because the induction heater might be operated from either 115 or 220 V sources. A modest heat sink is required because 100 W is dissipated in the power FETs at a full output power of 500 W.

120 kHz INDUCTION HEATER (500 W)



TMOS Sonar Transducer/Switch

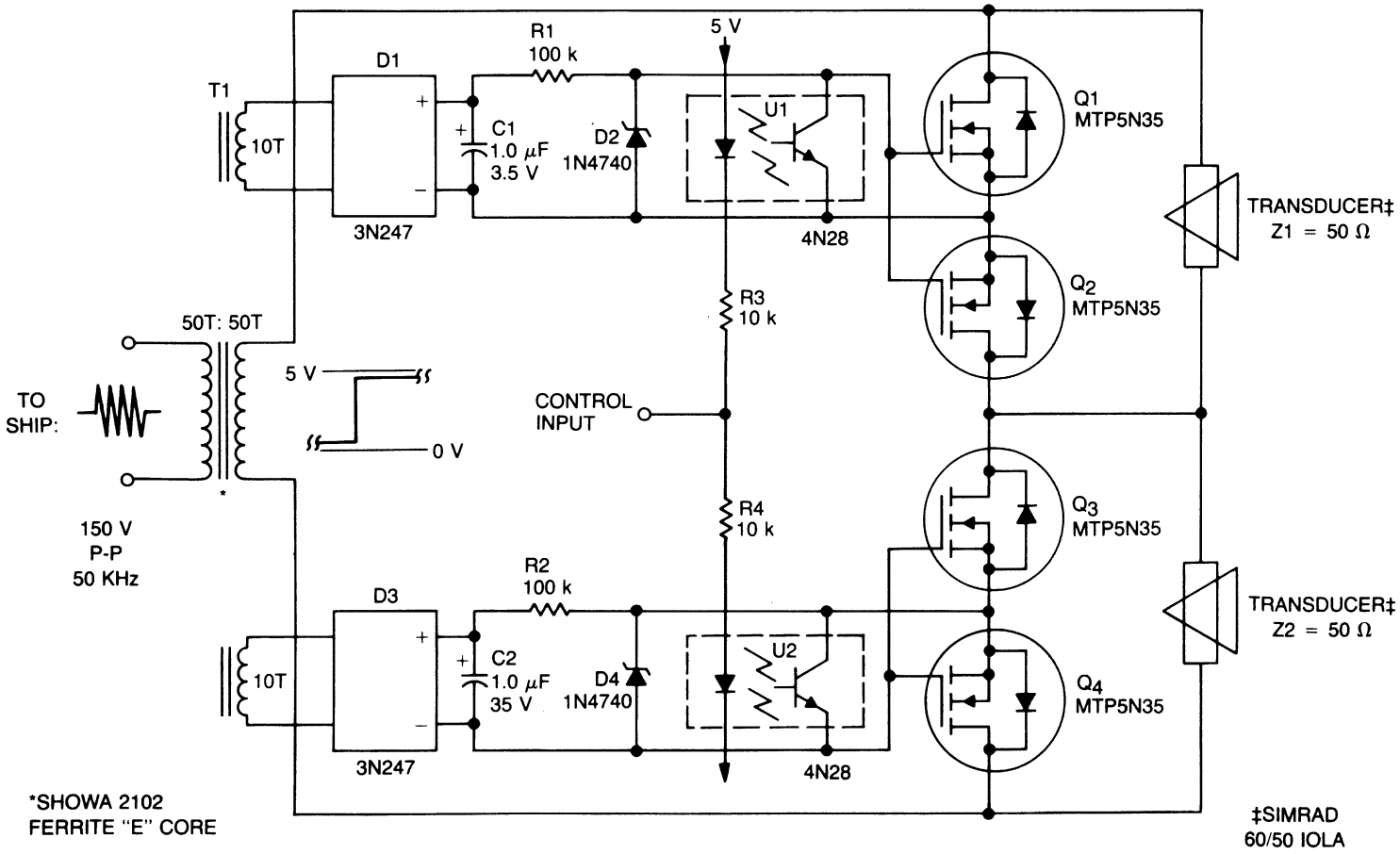
Russell Thynnes, *Seattle, WA*

Submersible sonar positioning apparatus generally consists of dual-opposed ultrasonic transducers, alternately excited, with return signals processed and displayed for observation and measurement. Typical transmitter frequencies range from 50 to 200 kHz and pulse widths may be varied from 0.3 to 5 msec, depending on depth and resolution requirements.

In operation, a pulse generated in the ship is sent to the Transducer/Switch via a coaxial transmission line. The TMOS Transducer/Switch accepts the pulses and alternately selects either of two transducers to transmit and receive sonar signals.

The input to the Transducer/Switch is transformer T1 that provides isolation and impedance matching. Turns ratio of the secondary windings depends on the peak-to-peak amplitude of the transmitter output into the specified load. The transmitted pulse that appears on the secondary winding charges capacitors C1 and C2 through bridge rectifiers D1 and D3. Zener diodes D2 and D4 limit TMOS gate bias to 12 V; R1 and R2 limit discharge current from C1 and C2.

The square wave control input is applied to opto-isolators U1 and U2 through resistors R3 and R4. If the control input is 0 V, U1 is activated, when it changes to +5 V, U2 is activated. When U1 is activated, it saturates and reduces the gate bias to zero, turning Q1 and Q2 OFF. Q3 and Q4 remain ON, effectively shunting transducer Z2. When U2 is activated, it saturates and reduces the gate bias to zero, turning Q3 and Q4 OFF. Q1 and Q2 remain ON, effectively shunting transducer Z1.



Magnet Current Regulator

Steven Young, *Menlo Park, CA*

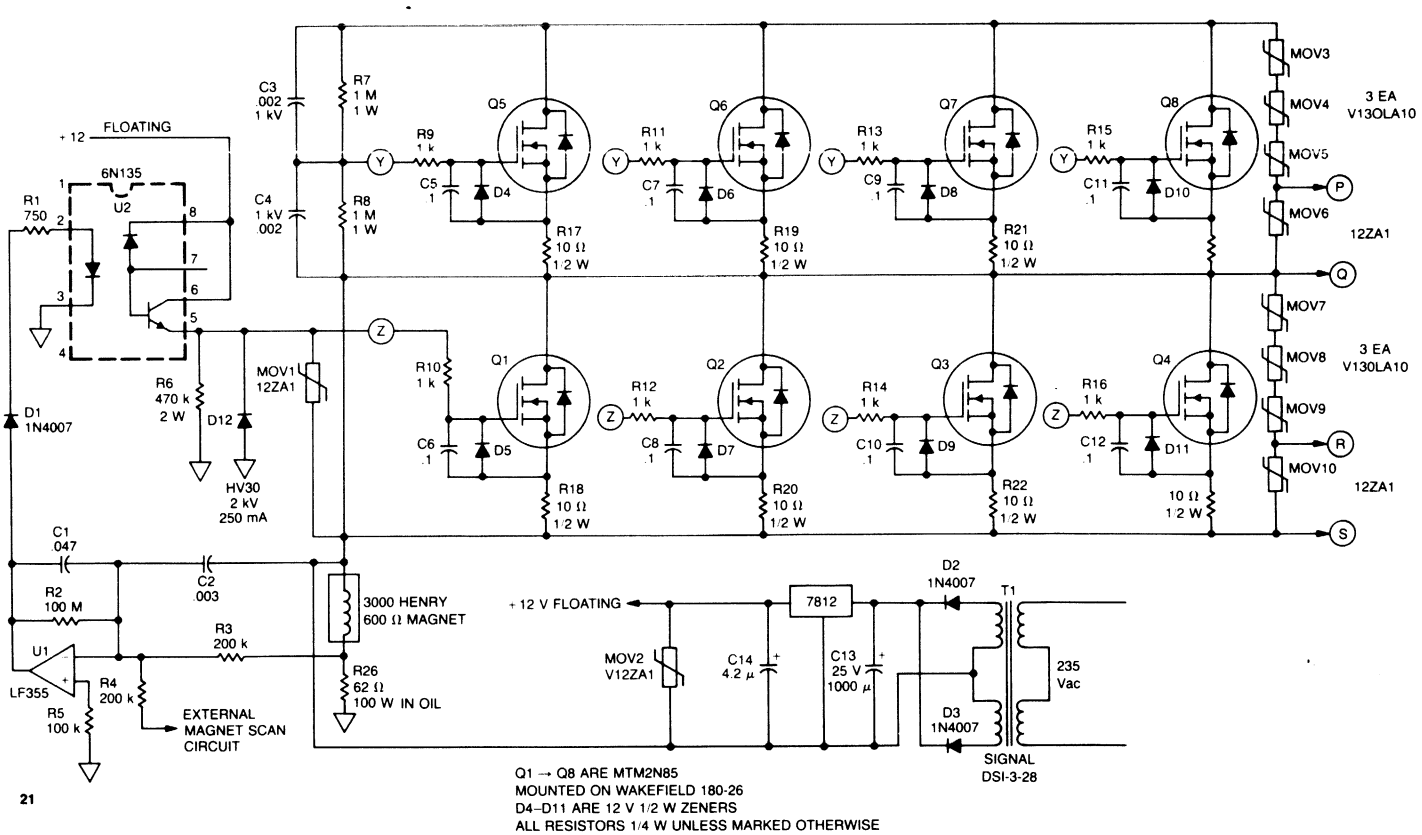
Eight TMOS devices replaced three vacuum tubes ($1000 a matched set) in a magnet current regulator of a 20-year old mass spectrometer. Power MOSFETs were used because they are cost effective and reliable, and essentially no changes were required for the 1200-V, 1-A power supply and high impedance electromagnet. Previous designs, using bipolar transistors, required 20 devices and failed frequently.

The magnet is 600Ω and 3000H; it requires 700 V for full field of 16,000 gauss and is scanned slowly from high field to low field about once a minute.

Q1 through Q8 form a "totem pole" regulator with Q1-Q4 as a master and Q5-Q8 as a slave. Current passing through the magnet generates a feedback voltage across the R26 reference resistor. This feedback voltage is compared with the programming voltage by U1, which in turn drives the opto-isolator (U2) that varies the gate bias to Q1-Q4.

Because of the "totem pole" arrangement, the inductance of the magnet and the high drain-to-gate capacitance of Q1-Q8, serious oscillation problems can be encountered. This is solved by shunting a 0.1 mfd capacitor from source-to-gate of each TMOS device. It slows down the circuit, but is no problem in this application.

An optional digital protection circuit monitors the magnet current regulator and shuts OFF the 235 V ac if there is a problem.



200 V DC Piezoelectric Gas Valve Switch

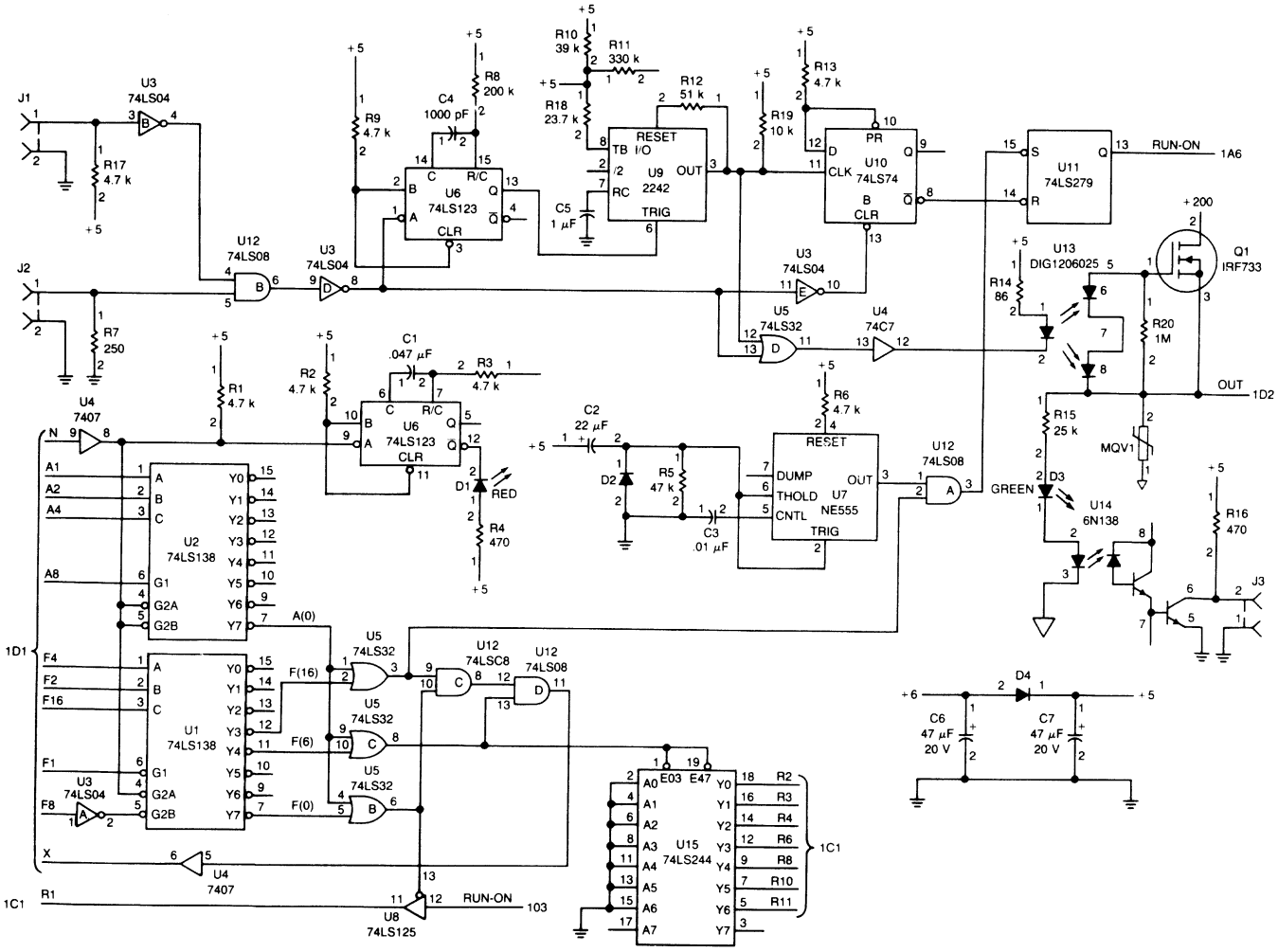
Mark Strauch, *Livermore, CA*

Under TTL command, this module switches 200 V to a piezoelectric valve that controls the supply of gas to a neutral beam accelerator. The switch module consists of three sections as outlined in the schematic: 1) CAMAC interface, 2) power switching, 3) run-on protection.

The CAMAC interface, ICs U1 through U6, U8 and U12, is an IEEE standard. It provides an interface between an "instruction bus" and the module. Only two commands are recognized: READ FAULT and RESET FAULT. These circuits are not involved in power switching.

U13 is a opto-isolator with a single LED and two isolated photosensors that are externally connected in series; it provides a floating gate drive signal to Power FET, Q1. When turned ON, Q1 sources 200 V off the board (accelerator connection "OUT") to drive a piezoelectric valve. MOV1 provides needed transient protection because the distance between Q1 and the load is over 200 feet. Isolator U14 drives provides an isolated output that indicates Q1's operation. The 200 V supply is completely isolated from control power.

For safety considerations, it is important that the module protect itself against timing system failures that may result in run-on (continuous gas flow). Therefore, input J1 is an enable signal and J2 is the timing system signal. ICs U6 and U9 through U11 qualify the timing signal against an internally triggered timer. Timing requests in excess of internal limits result in termination of drive to Q1.



PWM Speed Control and Energy-Recovering Brake

L. K. Palmer, *Las Vegas, NV* *Third Prize Winner*

Introduction of high current Power FETs and PWM control ICs has simplified the design and implementation of high efficiency dc motor speed controls. Higher di/dt ratings, current sharing ability and no need for commutation circuits make these Power FET families preferred over SCRs in many motor drive applications.

This circuit carries the concept of high efficiency PWM speed controls one step further by using the main drive motor as a generator/brake to recover battery charge during vehicle braking. When this is done, it can increase the overall range and efficiency of an electric vehicle.

In the accelerate mode, Q1-Q3 receive gate pulses from U1, an on-line, current mode, PWM controller IC. Assuming negligible effects of R, when Q1-Q3 turn ON, current I1 builds up through the motor at a rate of:

$$\frac{dI_1}{dt} = \frac{V_B - V_A}{L_A}$$

where V_A = Battery voltage
V_B = Motor's back EMF
L_A = Motor inductance in Henries

Motor current and torque continue to rise until the voltage on the I_{sense} line is greater than I_{reset}, as determined by the speed potentiometer. At this time, Q1-Q3 are switched OFF, current I_2 begins to flow and decreases at a rate of:

$$\frac{dI_2}{dt} = \frac{V_A}{L_A}$$

until the next clock period begins. The driving torque produced by the motor then becomes proportional to the duty cycle of Q1-Q3.

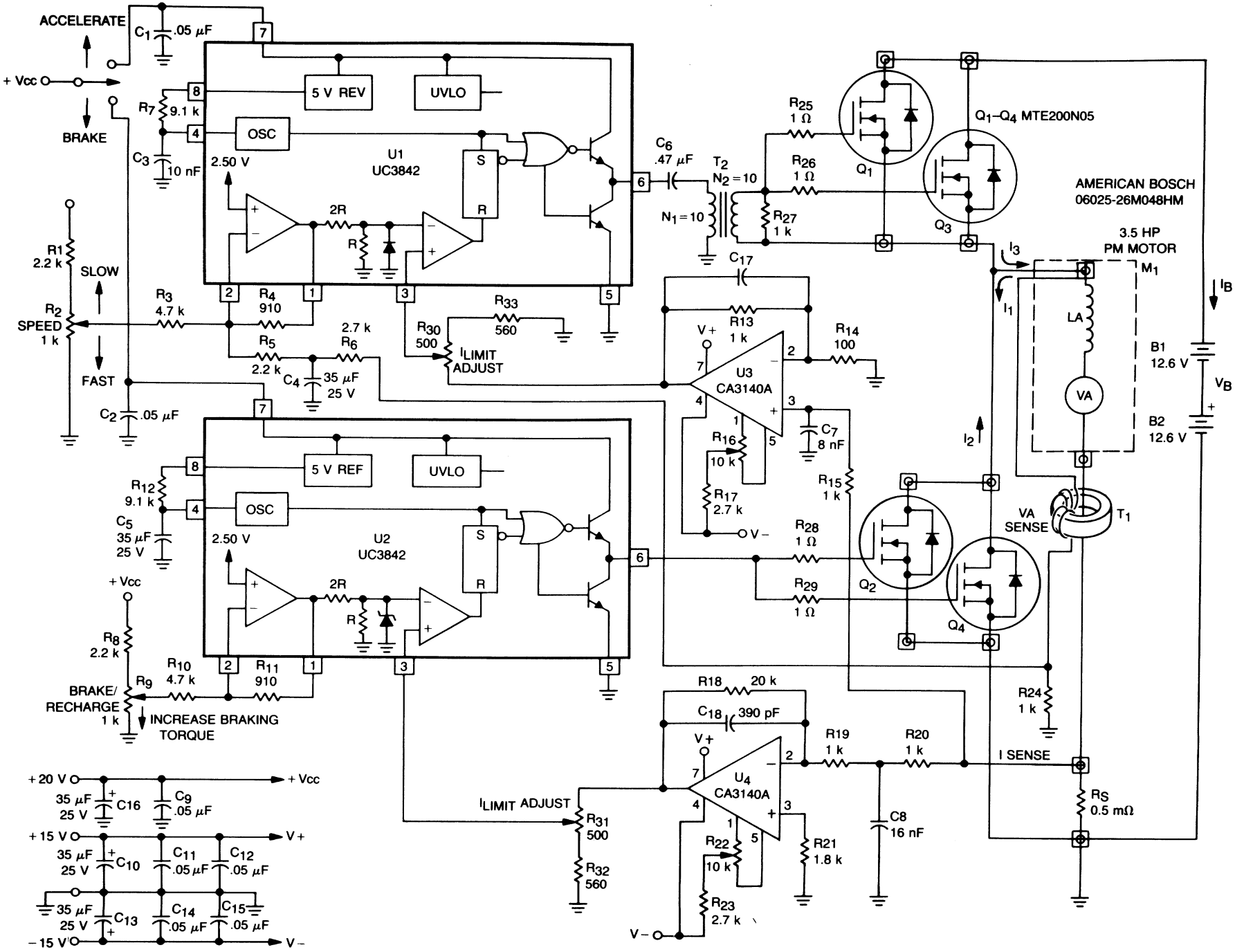
As vehicle braking occurs, the accelerate PWM IC (U1) is switched OFF and the braking PWM IC (U2) and Q2-Q4 are switched ON. During this time, the back EMF source voltage causes current I_3 to begin to flow at the rate of:

$$\frac{dI_3}{dt} = \frac{V_A}{L_A}$$

Current I_3 continues to rise until I_{sense} is greater than I_{reset}. Now, Q2-Q4 is switched OFF and IB is forced to flow back into the storage battery, thus energy is recovered.

The braking torque produced by the motor is proportional to the average reverse current that flows through the motor on the duty cycle of Q2-Q4. Braking force can continue until $\omega_A = 0$.

For reliable performance, voltage supplies should be independent of the main battery voltage.


ACCELERATE
+ Vcc
BRAKE
C1 .05 µF
R7 9.1 k
C3 10 nF
5 V REV
UVLO
OSC
2.50 V
U1
UC3842
2R
R
S
R
R1 2.2 k
SLOW
R2 SPEED 1 k
FAST
C2 .05 µF
R3 4.7 k
R4 910
R5 2.2 k
C4 35 µF 25 V
2.7 k
R6
R30 500
ILIMIT ADJUST
R33 560
C6 .47 µF
T2
N2 = 10
N1 = 10
R25 1 Ω
R26 1 Ω
R27 1 k
Q1
Q1–Q4 MTE200N05
Q3
AMERICAN BOSCH
06025-26M048HM
3.5 HP
PM MOTOR
M1
I3
I1
LA
VA
B1 12.6 V
B2 12.6 V
IB
VB
C17
R13 1 k
R14 100
V+
U3
CA3140A
V–
R16 10 k
R17 2.7 k
C7 8 nF
R15 1 k
I2
VA SENSE
T1
R28 1 Ω
R29 1 Ω
Q2
Q4
R12 9.1 k
C5 35 µF 25 V
U2
UC3842
+ Vcc
R8 2.2 k
BRAKE/ RECHARGE 1 k
R9
R10 4.7 k
R11 910
INCREASE BRAKING TORQUE
R18 20 k
C18 390 pF
U4
CA3140A
R19 1 k
R20 1 k
I SENSE
R24 1 k
RS 0.5 mΩ
ILIMIT ADJUST
R31 500
R32 560
R22 10 k
R23 2.7 k
R21 1.8 k
C8 16 nF
+ 20 V
C16 35 µF 25 V
C9 .05 µF
+ 15 V
C10 35 µF 25 V
C11 .05 µF
C12 .05 µF
C13 35 µF 25 V
C14 .05 µF
C15 .05 µF
– 15 V
V+
V–

FC0181

Back EMF PM Motor Speed Control

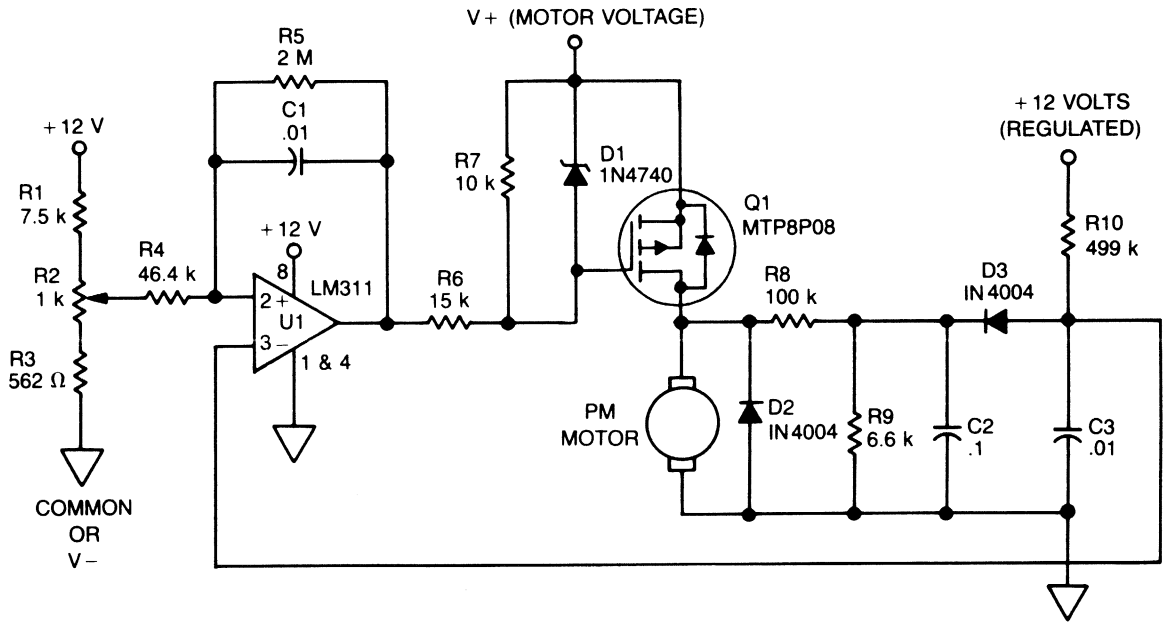
Jim Alleman, *Houston, TX*

Use of power MOSFETs allows a direct interface between logic and motor power, which permits circuit simplicity as well as high efficiency. This speed control circuit can be packaged on a 22-pin, double-sided, 3.5 X 4-in. p.c. board.

A 12 V control supply and a TRW BL11, 30 V motor are used; with minor changes other motor and control voltages can be accommodated. For example, a single 24 V rail could supply both control and motor voltages. Motor and control voltages are kept separate here because CMOS logic is used to start, stop, reverse and oscillate the motor with a variable delay between motor reversals.

Motor speed is established by potentiometer R2, which applies a corresponding dc voltage to the + input of comparator U1, whose output is then applied to TMOS device MTP8P08 (Q1). Zener diode D1 limits the drive to Q1. The output of Q1 drives the permanent magnet motor.

Back EMF is obtained from the motor via the network consisting of R8, R9, R10, C2, C3 and D3; it is applied to – input of comparator U1.

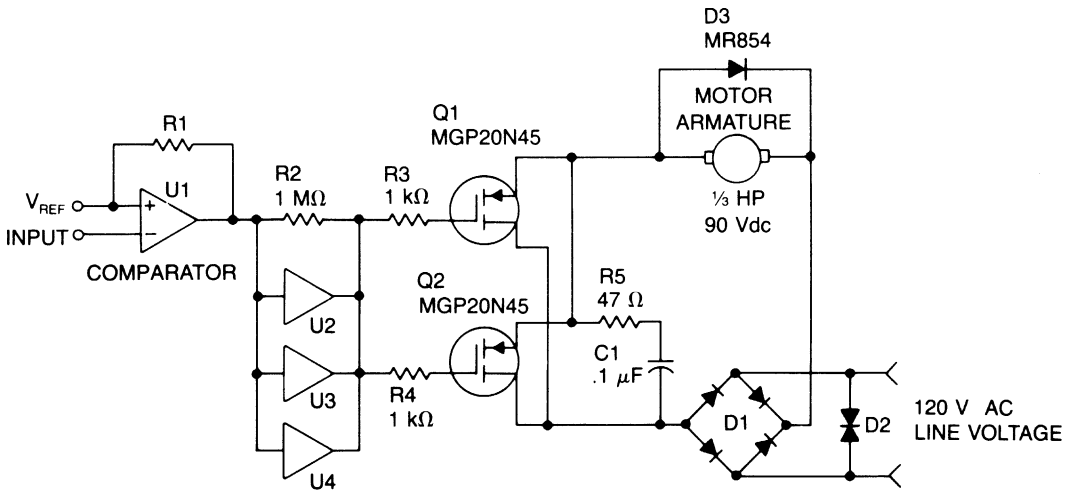


PWM Motor Speed Control

Robert Ritzsche, *Chaska, MN*

Speed control is accomplished by pulse width modulating the gates of two MGP20N45 TMOS devices. Therefore, motor speed is proportional to the pulse width of the incoming digital signal, which can be generated by a microprocessor or digital logic.

The incoming signal is applied to comparator U1, then to paralleled inverters U2, U3 and U4 that drive the two TMOS devices, which, in turn, control power applied to the motor armature. Bridge rectifier D1 supplies full-wave power that is filtered by R5 and C1. Free-wheeling diode D3 (MR854) prevents high voltage across Q1 and Q2. A back-to-back zener diode, D2, protects against transients and high voltage surges.



High Efficiency, Off-Line Switching Power Supply

Marek Gajenski, *Woodland Hills, CA Third Prize Winner*

This multi-output, off-line SMPS uses a full-cycle, push-pull 30 kHz converter preceded by a buck-type pre-regulator that is duty cycle modulated at 200 kHz. Efficiencies of 90% may be achieved with this circuit.

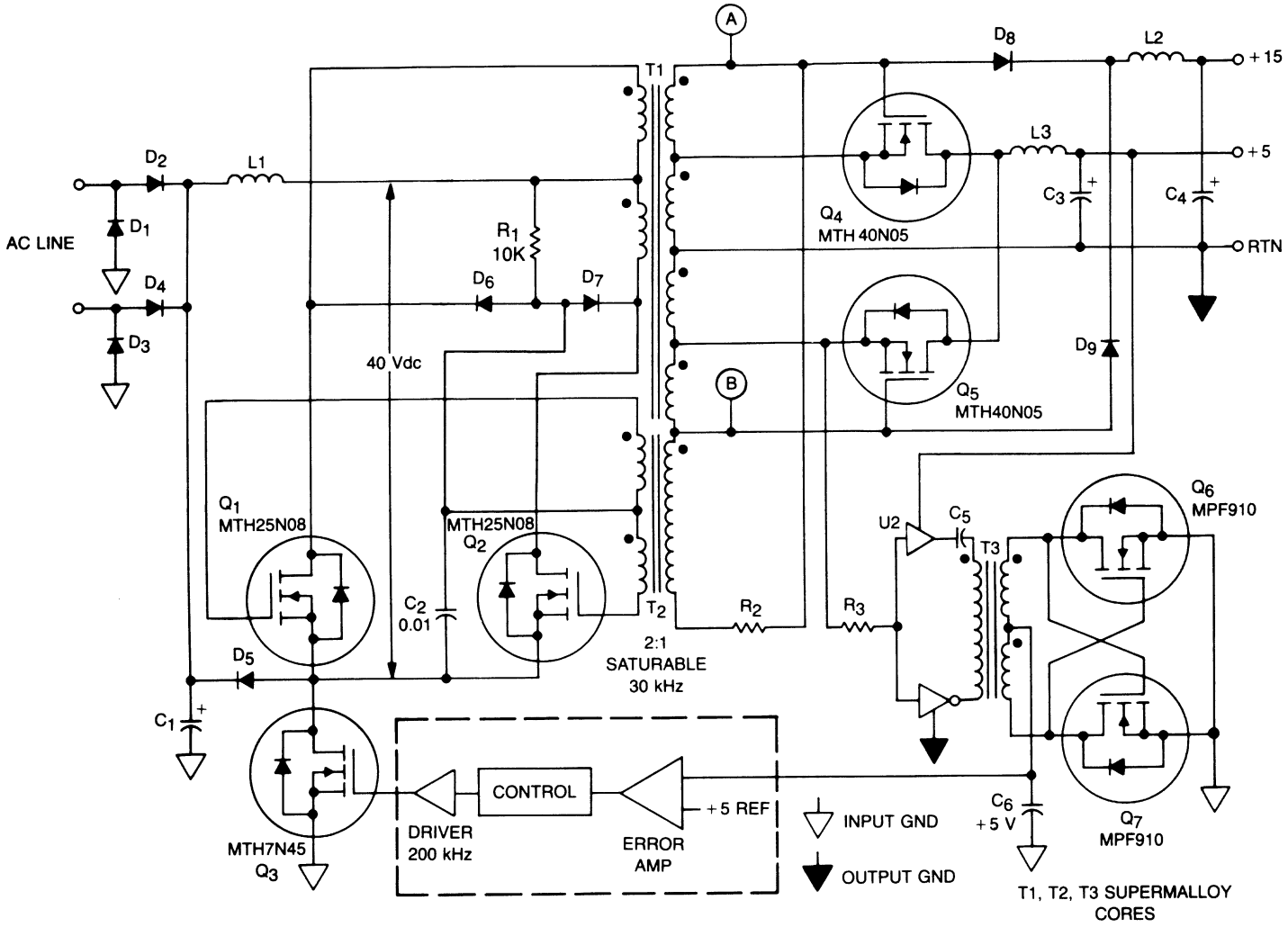
The power supply has a number of significant features. Inherently low output noise and low output impedance of the full-cycle converter allows use of much smaller filter capacitors than those of a duty cycle modulated converter. Redundant shutdown prevents abnormal behavior at both output and input in case of switching transistor failure. Core saturation of T1 is completely eliminated by free-running switching that ensures automatic duty cycle symmetry compensation, which accommodates even badly mismatched switching transistors. Using diodes D6 and D7 to hold the center tap of driver transformer T2 close to the converter's return potential eliminates cross-conduction inducing gate drive overlap. And, no snubber is required.

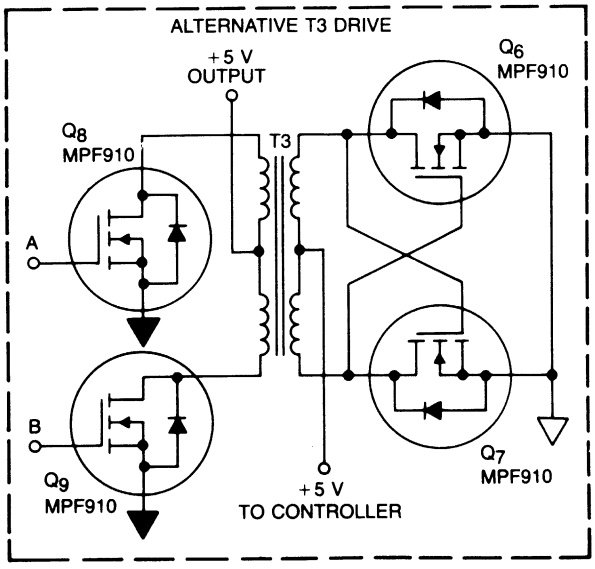
Absence of a large filter capacitor after the buck regulator's inductor (L1) prevents excessive energy storage in T1's inter-winding and intra-winding capacitance. At the same time, it does not add a second-order pole at lower frequencies, which simplifies loop compensation. Also, the load capacitance is transformed into the primary and serves as an energy storage element during the OFF cycle.

Because of its superior ON-resistance and faster switching times, the buck pre-regulator, Q3, uses an N-Channel MTH7N45 rather than a P-Channel device. Referred to ground, it is conveniently driven by a simple 4050 CMOS driver. For higher current applications, a parallel connection of two MTH7N45s may be used, which is still less costly than an equivalent TO-3 device.

Q4 and Q5 form a synchronous rectifier for the +5 V output. Up to 20 A, these devices offer lower dynamic and static losses than conventional Schottky diodes. For up to 50 A, the MTE200N05 can be used; it has only 9 mv On-resistance and is better than equivalent Schottky diodes.

Input/output ground isolation for the error voltage is accomplished with a small transformer, T3, using a 4041 push-pull driver on its primary side and a synchronous rectifier consisting of MPF910 TMOS Power FETs (Q6 and Q7). Unlike opto-isolators, the transfer function of such a module is insensitive to temperature and production tolerances and remains very close to unity, which introduces negligible error to output voltage tolerance.


AC LINE
D1
D2
D3
D4
L1
T1
R1
10K
D6
D7
40 Vdc
A
B
D8
L2
+15
L3
+5
C3
C4
RTN
Q4
MTH 40N05
Q5
MTH40N05
D9
Q1
MTH25N08
MTH25N08
Q2
C2
0.01
T2
2:1
SATURABLE
30 kHz
R2
R3
U2
C5
T3
Q6
MPF910
Q7
MPF910
D5
C1
MTH7N45
Q3
DRIVER
200 kHz
CONTROL
ERROR
AMP
+5 REF
INPUT GND
OUTPUT GND
C6
+5 V
T1, T2, T3 SUPERMALLOY
CORES


ALTERNATIVE T3 DRIVE
+5 V
OUTPUT
Q6
MPF910
Q8
MPF910
T3
A
B
Q9
MPF910
Q7
MPF910
+5 V
TO CONTROLLER

Complementary Output Variable Frequency Inverter

Steve Bennett, *Two Rivers, WI*

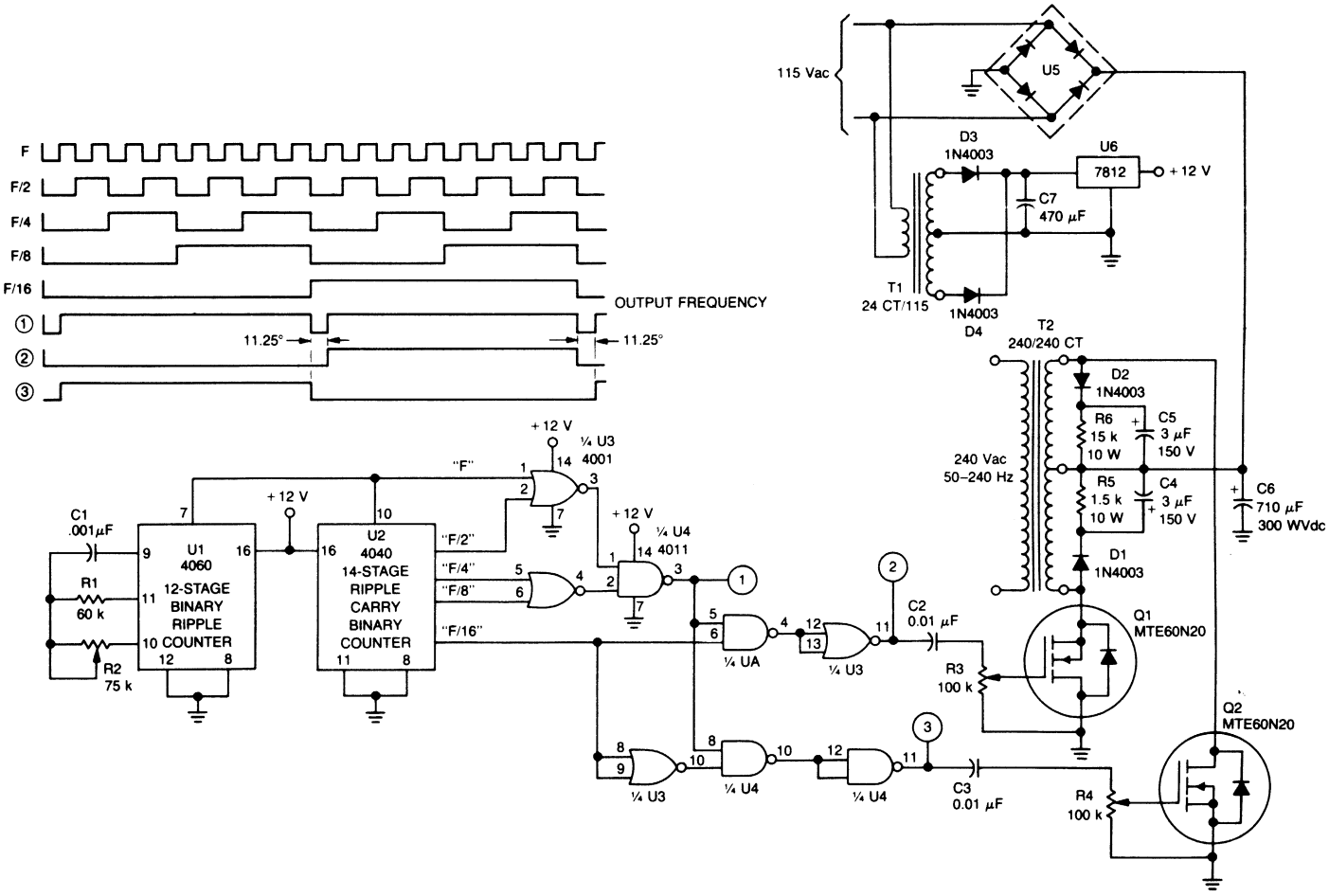
This circuit generates complementary output signals from 50 to 240 Hz. Digital control of timing ensures a separation of 10 to 15° between the fall time of one output and the rise time of the complementary output.

The digital portion of this inverter (U1 to U4) controls the drive to Q1 and Q2, both MTE60N20 TMOS devices. These devices are turned ON alternately with 11.25° separation between complementary outputs.

A + 12 V supply for CMOS gates U1 to U4 is developed by transformer T1, D3 and D4, C7, and U6. The power supply for the TMOS frequency generator is derived from diode bridge, U5, and capacitor C6; it is applied to the center tap of T2.

U1 is a 4060 12-stage binary ripple counter that is used as free-running oscillator; its frequency of oscillation is: 1/2.2 C1R2. The output of U1 is applied to U2, a 14-stage binary ripple counter that provides square wave outputs of 1/2, 1/4, 1/8 and 1/16 of the clock frequency. These signals are combined in U3 and U4 to provide complementary drive for Q1 and Q2.

Outputs from U3 and U4 are ac-coupled to Q1 and Q2 via C2 and C4, respectively. R3 and R4 adjust the gate drive to Q1 and Q2. Q1 and Q2 alternately draw current through opposing sides of the primary to synthesize an ac input voltage at a given frequency. Only one side of the primary of T2 is driven at one time, so maximum power output is half of the transformer rating.



Self Oscillating, Flyback Switching Converter

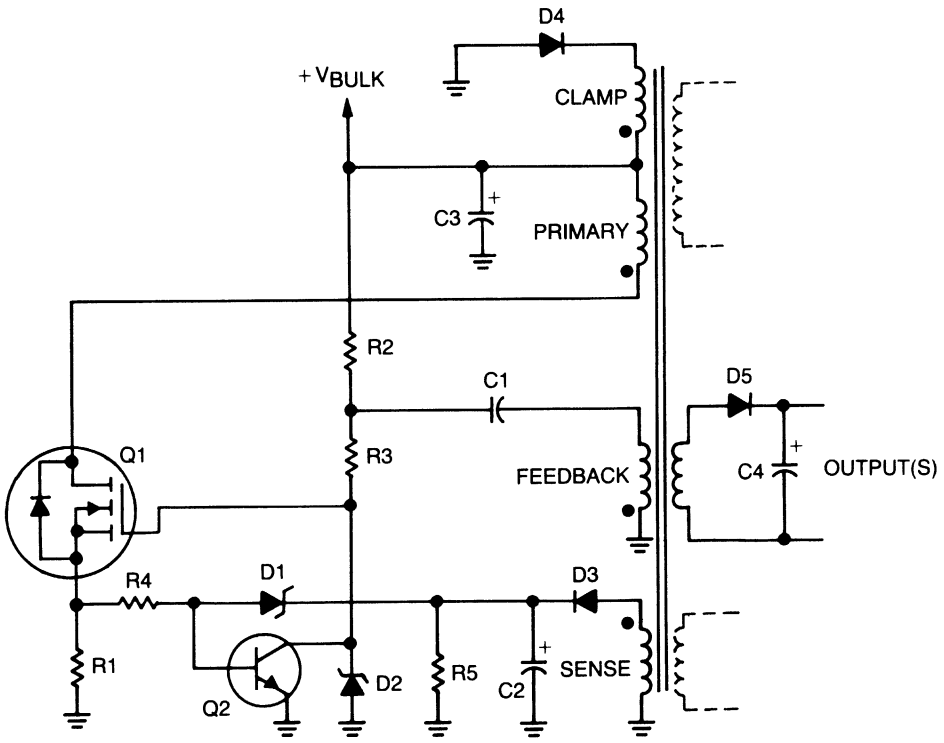
Douglas Glenn, *Lewisburg, TN*

In-phase transformer windings for the drain and gate of TMOS Power FET Q1 cause the circuit to oscillate. Oscillation starts when the feedback coupling capacitor, C1, is charged from the supply line via a large resistance, R2. R3 limits the collector current to Q2. During "pump-up", the ON time is terminated by Q2, which senses the ramped source current of Q1. C1 is charged on alternate half-cycles by Q2 and forward-biased zener D2.

When the regulated level is reached, forward bias is applied to Q2, terminating the ON time earlier at a lower peak current. When this occurs, the frequency increases in inverse proportion to current, but the energy per cycle decreases in proportion to current squared. Therefore, the total power coupled through the transformer to the secondary is decreased.

Regulation is provided by taking the rectified output of the sense winding and applying it as a bias to the base of Q2 via zener D1. The collector of Q2 then removes drive the gate of Q1. Therefore, if the output voltage should tend to increase, Q2 removes the drive to Q1 earlier, shortening the ON time, and the output voltage will remain the same.

Dc outputs are obtained by merely rectifying and filtering secondary windings, as done by D5 and C4.



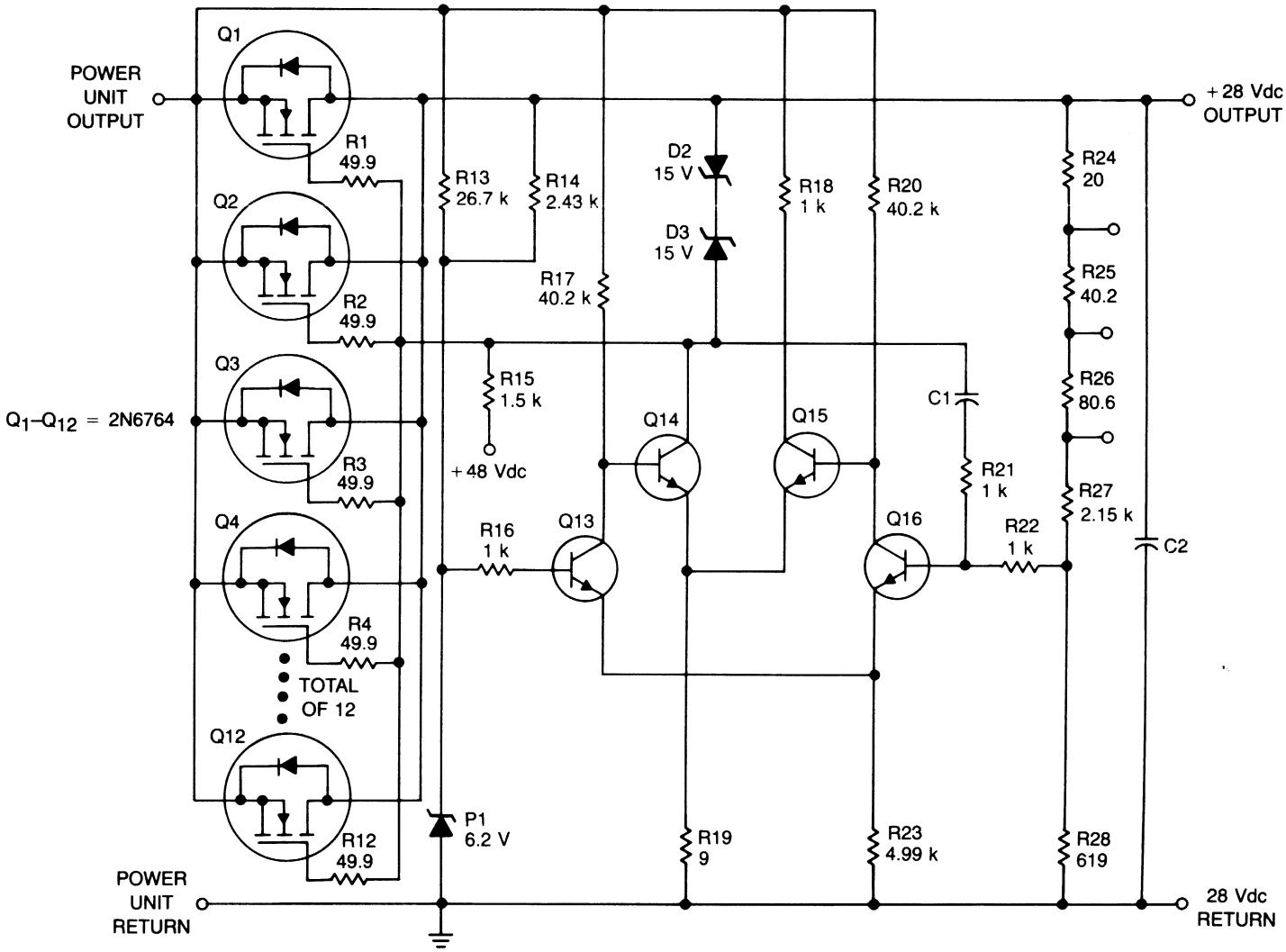
Radiation-Hardened, 125 A Linear Regulator

Tom R. Seaton, *Portland, OR*

Intended for extreme temperature, radiation-hardened environments, this linear supply is capable of supplying 28 V dc at 125 A from an ac-driven power unit. A linear approach was chosen for its inherent low ripple and noise, simplicity, reliability, wide bandwidth and also to provide the instantaneous current required to clear shorts.

In operation, power supply output voltage is sensed by the voltage divider consisting of R24 to R28 and fed to one input of a discrete differential amplifier composed of Q13 through Q16. The other input of the amplifier is connected to a radiation-hardened zener diode, D1. Local feedback using R21 and C1 produces gain and phase shift that are independent of individual component parameters, which provides stable operation into the required loads.

Clamped by back-to-back zener diodes (D2 and D3), the differential amplifier drives the gates of the 12 paralleled TMOS devices through 49.9 Ω series resistors, which eliminate high frequency oscillations. The large number of MOSFETs insures sufficient current to clear output short circuits even under high temperature where their internal resistance increases and current-handling capacity is reduced. To insure reliable turn-on of the TMOS devices under all conditions, drive circuits are powered by an external +48 V dc supply. In this way, TMOS gates can be driven to +15 V dc relative to their sources. If the circuit is subjected to radiation, the gate threshold voltage of the TMOS becomes more negative, and can even reverse polarity with sufficient dosage. To handle this situation, the TMOS gates can be driven to −15 V dc.



Low Cost, Very Low Dropout Linear Regulator

Aubrey Elms, *Marlboro, MA*

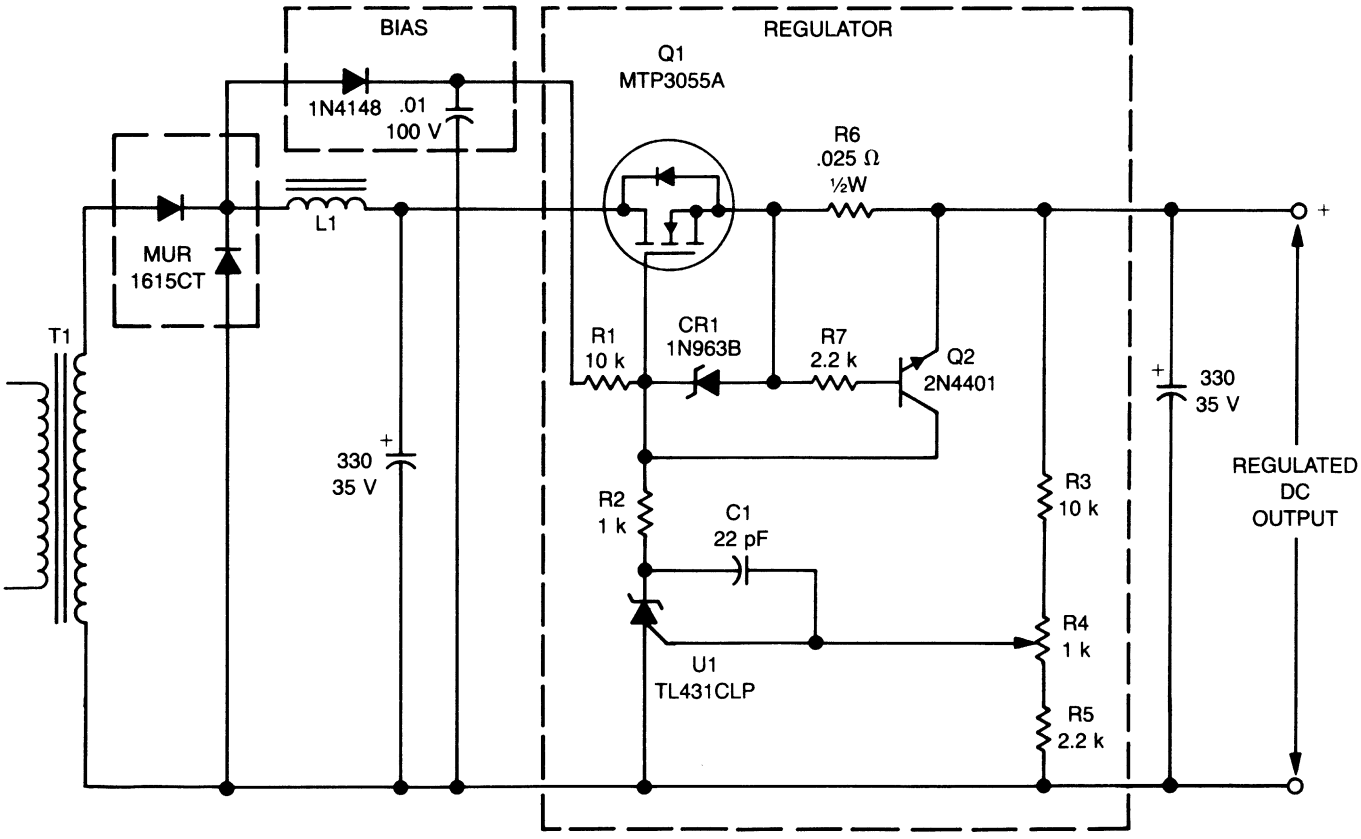
Linear power supplies are especially well-suited as post regulators in switcher designs. Performance of these linear supplies can be enhanced by using a power MOSFET series regulator, taking advantage of their very low dropout voltage and very low bias current requirements. Other factors, such as regulation, ripple rejection and transient response are equivalent to or better than the performance of conventional bipolar series pass transistors. In the circuit shown, circuit simplicity, small size and cost round out its features.

This linear post regulator provides 12 V at 3 A. It employs a TL431 reference (U1) which, without additional amplification, drives the gate of the TMOS MTP3055A (Q1) series pass regulator. Bias voltage is applied through R1 to Q1's gate, which is protected against overvoltage by diode CR1. Frequency compensation for closed loop stability is provided by C1.

Q1 was selected for a low rDS(ON) within the required voltage and current ratings. Any type of MOSFET can be chosen, but the best performance can be obtained from a device that is optimized for low ON resistance at low operating voltages. The TL431 shunt regulator, in a TO-92 package, is chosen for U1, considerably simplifying the design. R6, R7 and Q2 are optional; they can be added whenever peak current limiting is required.

Key performance features are:

Dropout voltage	0.6 V
Line regulation	±5 mV
Load regulation	10 mV
Output ripple	10 mV pk-pk



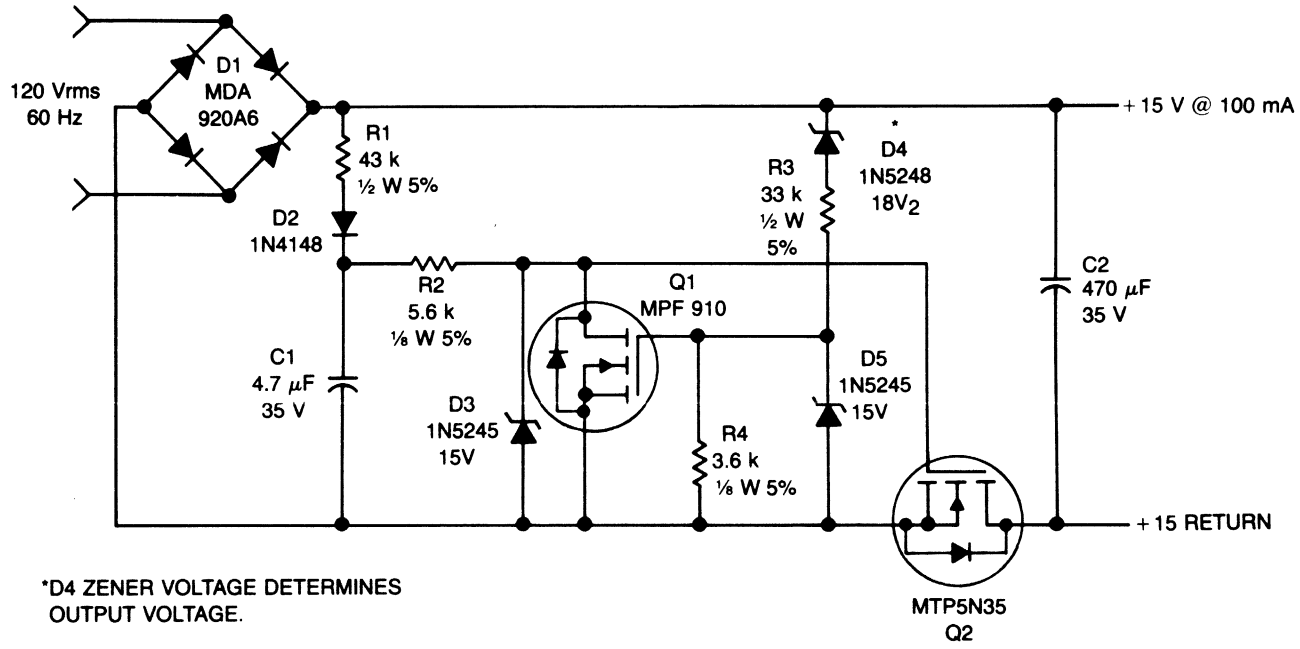
1.5 W Offline Converter

Woody Skelton, *Boulder, CO*

This non-isolated, unregulated, minimum component converter fills the void between low power zener regulation and the higher power use of a 60 Hz input transformer. It is intended for use where a non-isolated supply is safe. Commercial uses could include digital clocks and timers, NiCad battery chargers, and battery eliminaters for small radios, calculators and toys. Industrial uses could include delay timers, digital indicators and low power controls with opto-isolated or relay outputs.

The circuit operates by conducting only during the low voltage portion of the rectified sine wave. R1 and D2 charge C1 to approximately 20 V, which is maintained by Q1. This voltage is applied to the gate of Q2, turning it ON. When the rectified output voltage exceeds the zener voltage of D4, Q1 turns ON, shunting the gate of Q2 to ground, turning it OFF.

MOSFETs allow this circuit to function with greater efficiency than bipolar transistors and permit a lower component count. The slow switching ramps of this circuit can best be handled by MOSFETs.



High Voltage Bucking Regulator

Jim Hagerman, *Maynard, MA*

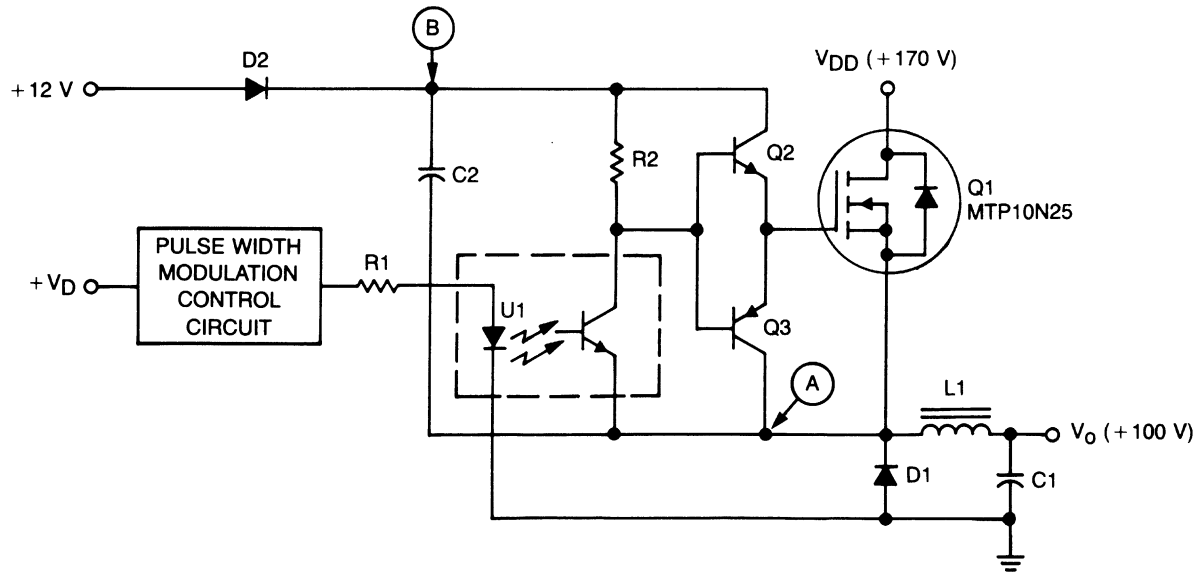
This circuit is basically the classic bucking regulator, except it uses a TMOS N-channel Power FET for the chopper and creates its own supply for the gate control.

The pulse width modulator can be just about any standard IC or circuit available for this purpose. Its output pulse drives the LED side (via a current limiting resistor) of opto-isolator U1. This isolation is necessary because the gate drive circuit power supply goes up and down with the voltage at point A.

The unique aspect of this circuit is how it generates a separate supply for the gate circuit, which must be greater than V_{DD}. When power is applied, C2 charges up, through D2, to +12 V. At this time, Q1 is OFF and the voltage at point A is just below zero. When the pulse modulated signal is applied, the opto-isolator transistor, Q2 and Q3 supply a signal to Q1 that turns it ON. The voltage at point A then goes to V_{DD}, C2 back-biases D2, and the voltage at point B goes to 12 V above V_{DD}.

After Q1 is turned ON, current starts to flow through L1 into C1, increasing until Q1 turns OFF. The current still wants to flow through L1, so the voltage at point A moves toward negative infinity, but is clamped by D1 to just below zero. Current flows less and less into C1 until Q1 turns ON again. Q2 and Q3 drive Q1's gate between the voltages at point A and B, which is always a 12 V swing, so V_{GS} max. is never exceeded.

For proper operation, the 12 V supply has to be established before the pulse width modulator signal is applied.



High Efficiency Flyback Voltage Converter

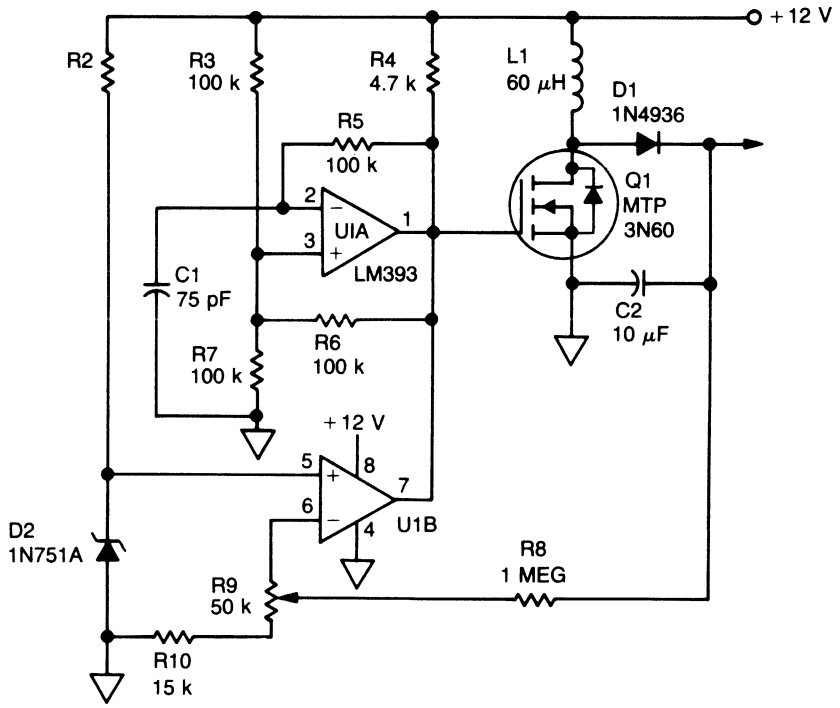
James Marshall, *Dallas, TX*

This flyback voltage converter provides a simple means for generating a regulated high voltage with few components and high efficiency. A great deal of circuit simplicity and efficiency is due to the use of a TMOS Power FET for Q1. Providing adequate drive current for a bipolar transistor would have required an additional stage with additional losses.

U1 is a dual voltage comparator with open collector outputs. The "A" side is an oscillator operating at 100 kHz and the "B" side is part of the regulation circuit that compares a fraction of the output voltage to a reference generated by zener diode D2.

The output of U1A is applied directly to the gate of Q1. During the positive half-cycle of the Q1 gate voltage, energy is stored in L1; in the negative half it is discharged into C2. A portion of the output voltage is fed back to U1B to provide regulation. The output voltage is adjustable by changing feedback potentiometer R9.

Component values shown produce a nominal 300 V output from a 12 V source. However, the circuit maximum output voltage is limited by R10; a lower value of R10 yields a higher output voltage. Output voltage is also limited by the breakdown values of Q1, L1, D1 and C2.



HV Regulator With Foldback Current Limiting

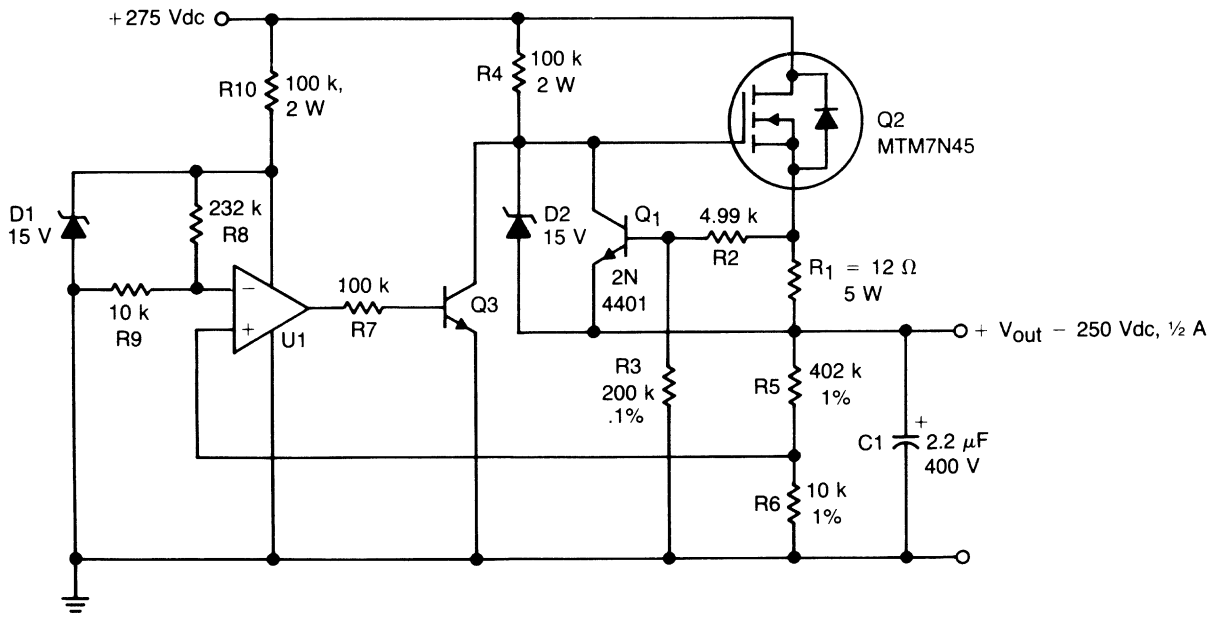
Larry Sears, *Cleveland, OH*

A TMOS MTM7N45 (Q2) is used as a series pass element in a linear high voltage supply that accepts +275 V unregulated and produces 250 V regulated with foldback current limiting.

A 15-V zener, D1, provides the dc reference for operational amplifier U1, whose other input is obtained from a fraction of the output voltage. U1 drives Q3, which drives the gate of Q2. Foldback current limiting is achieved by R1, R2, R3, R4, Q1 and D2. The formula to establish the current "knee" for limiting is:

$$I_{KNEE} = \frac{V_{OUT}(R2/R2+R3) + 0.5\ V}{R1}$$

Short circuit current is: $I_{SC} = \frac{0.5\ V}{R1}$



Uninterruptible Power Supply For Personal Computers

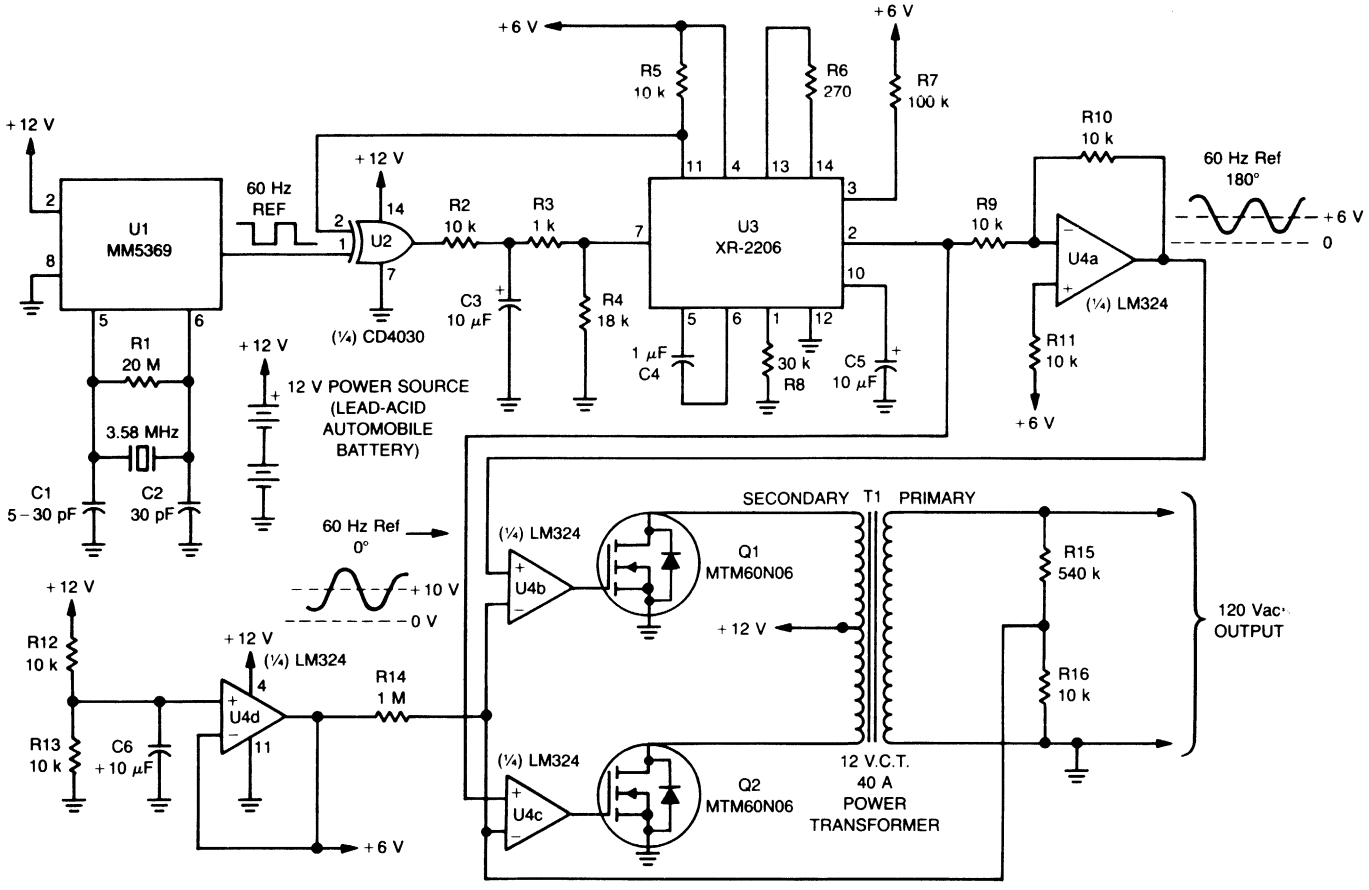
Bill Williams, *Columbus, OH*

A cost effective Uninterruptible Power System can be an important accessory for personal computers. Presented here is a low cost, stable, precisely 60 Hz, 120 VAC, 4 A UPS.

The UPS is basically an AC inverter that is power by a 12 V, lead-acid automobile battery. During power outages, it can supply several minutes of power for an average personal computer. It incorporates a crystal-controlled 60 Hz time base, so that a computer with a real time clock can maintain its accuracy. It isolates the ac line from the computer, so it can be used to operate sensitive electronic equipment on noisy power sources.

Two MTM60N06 Power FETs (Q1 and Q2) alternately switch current through a center-tapped 120 V-to-12 V filament transformer (T1) with its primary and secondary reversed. The 120 V output is compared with a 60 Hz reference in a closed-loop configuration that maintains a constant output at optimum efficiency.

A 60 Hz reference frequency is derived from a crystal oscillator and divider circuit, U1. An inexpensive 3.58 MHz color burst crystal provides the time base that can be accurately adjusted by C1. The 60 Hz output from U1 is applied to the exclusive-OR gate, U2, and then to the XR-2206 function generator (U3) that converters the square wave into a sine wave. U2 and U3 form a phase-locked loop that synchronizes the sine wave output of U3 with the 60 Hz square wave reference of U1. The sine wave is then inverted by op amp U4a, so that two signals 180 out of phase can be applied to U4b and U4c that drive Q1 and Q2. Due to the closed-loop configuration of the drive circuits, Q1 and Q2 conduct only during the upper half of the sine wave. Therefore, one TMOS device conducts during the first half of the sine wave and the other conducts during the second half.



High Efficiency, 80-Meter Amateur Radio Transmitter

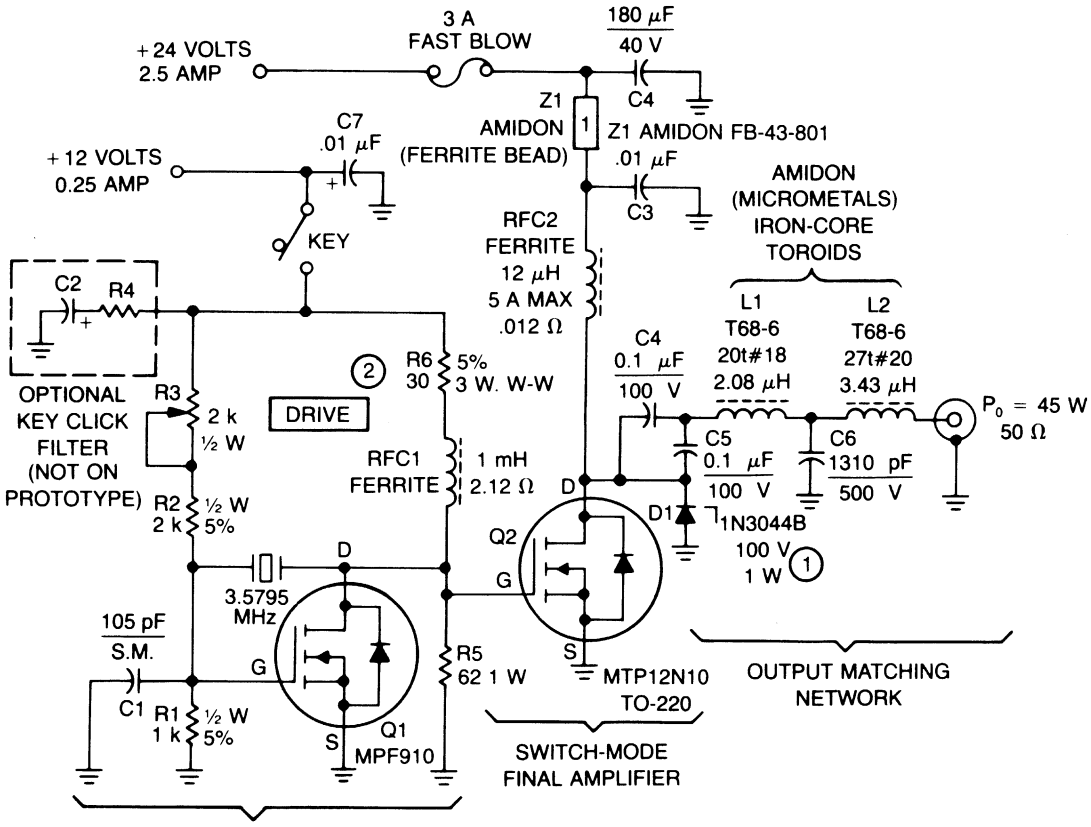
Robert G. Culter, *Beaverton, OR* *Second Prize Winner*

This transmitter consists of a keyed crystal oscillator/driver and a high efficiency final, each with a TMOS Power FET as the active element. Total parts costs are less than $20 and no special construction skills or circuit boards are required.

The Pierce oscillator is unique because the high C_{iss} of the final amplifier Power FET (700-1200 pF) is used as part of the capacitive feedback network. In fact, the oscillator will not work without Q2 installed. The MPF910 is a good choice for this oscillator because it is capable of driving the final amplifier in a switching mode while still retaining enough gain for oscillation.

To minimize cost, a readily-available color burst TV crystal is used as the frequency determining element for Q1.

An unusual 84% output efficiency is possible with this transmitter. Such high efficiency is achieved due to the TMOS Power FET's characteristics along with modification of the usual algorithm for determining output matching. Drain impedance is assumed to be: $R_o = (V_{cc})^2/2 \cdot P_o = (24)^2/2 \cdot 50 = 5.76\Omega$. We can assume the drain resistance is a factor of two higher due to conduction being cut off for a larger part of the cycle. Therefore, the matching network can be calculated for the case where the drain voltage is allowed to exceed Vcc by a considerable amount for part of the conduction cycle. The resulting efficiency exceeds the usually expected 50% from Class C operation.



1. Use Zener (100 V) with 100 V rated Q2. Zener not required with MTP8N18 or similar high-voltage part.
2. Adjust DRIVE for minimum oscillation delay on keying.

Double Sideband, Suppressed Carrier R.F. Modulator

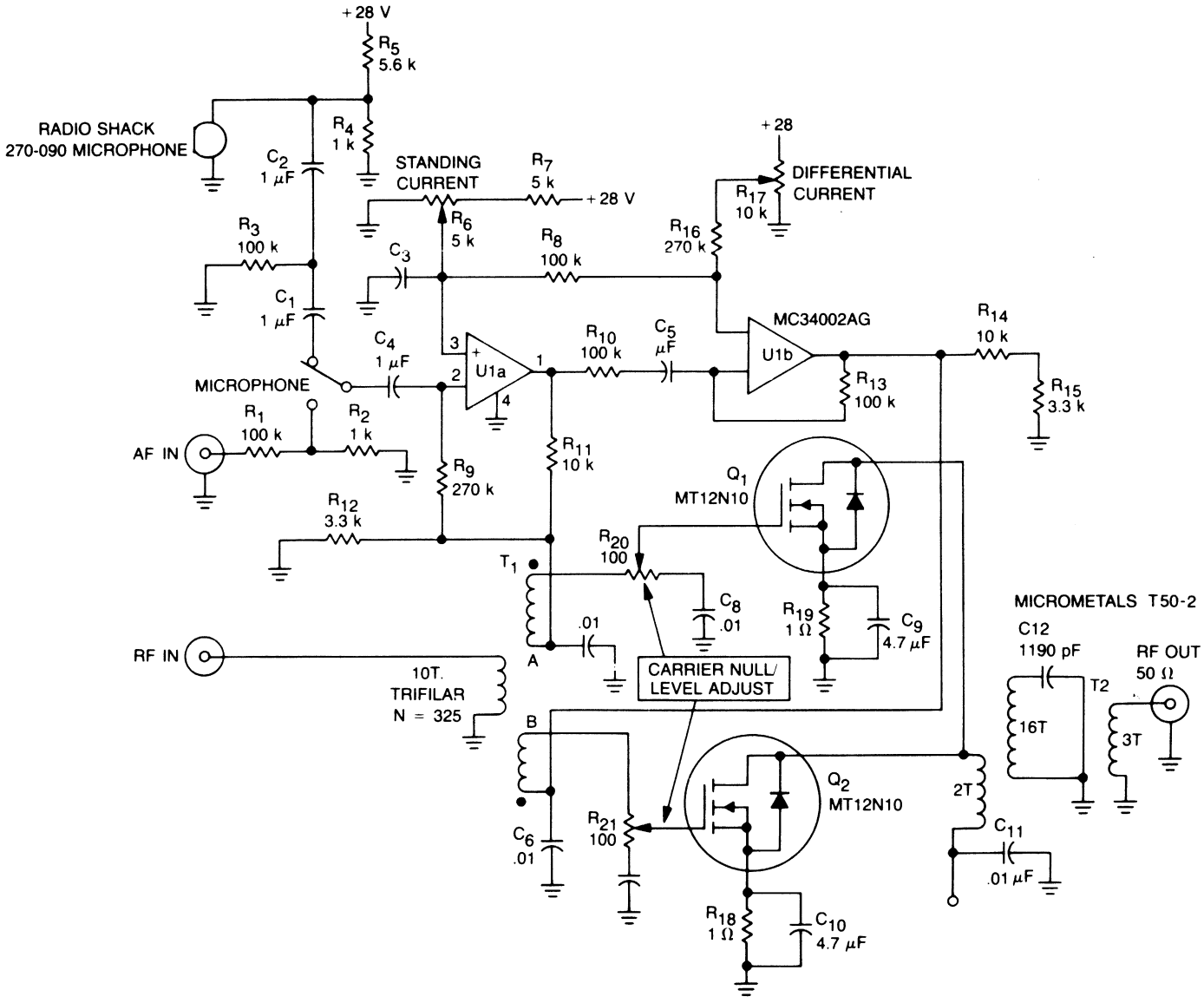
Larry Lockwood, *McMinnville, OR* *Third Prize Winner*

High power gain at both AF and RF frequencies are possible with TMOS Power FETs. In particular, RF applications can take advantage of the large SOA, which minimizes the concern for the harmful effects of reflected energy on the output devices. Furthermore, the linearity of Power FETs improves the modulation process.

An RF input is applied to the primary of T1, which applies equal amplitude, opposite phase RF drive for output FETs Q1 and Q2. With no AF modulation at points A and B, the opposite phase RF signals cancel each other and no output appears at the 50v output connector.

When AF modulation is applied to points A and B, a modulated RF output is obtained. DC stability and low frequency gain are improved by source resistors R18 and R19.

A phase inverter consisting of a dual op amp (U1a and U1b) produces the out-of-phase, equal amplitude AF modulation signals.



Low Distortion, High Power AM Transmitter Modulator

Fred Studenberg, *Melbourne, FL*

To meet worldwide regulations, transmitter modulation distortion must be less than 1% of the 80% modulation level. Therefore, it was decided to improve the existing modulator design to provide more margin for this adjacent channel power specification.

The original bipolar transistor design produced 2 V at an 8% duty cycle. Modulation below 2 V caused the modulator to be completely cut off for a number of cycles, which produced high order harmonics at the modulation valleys. The result was adjacent channel noise.

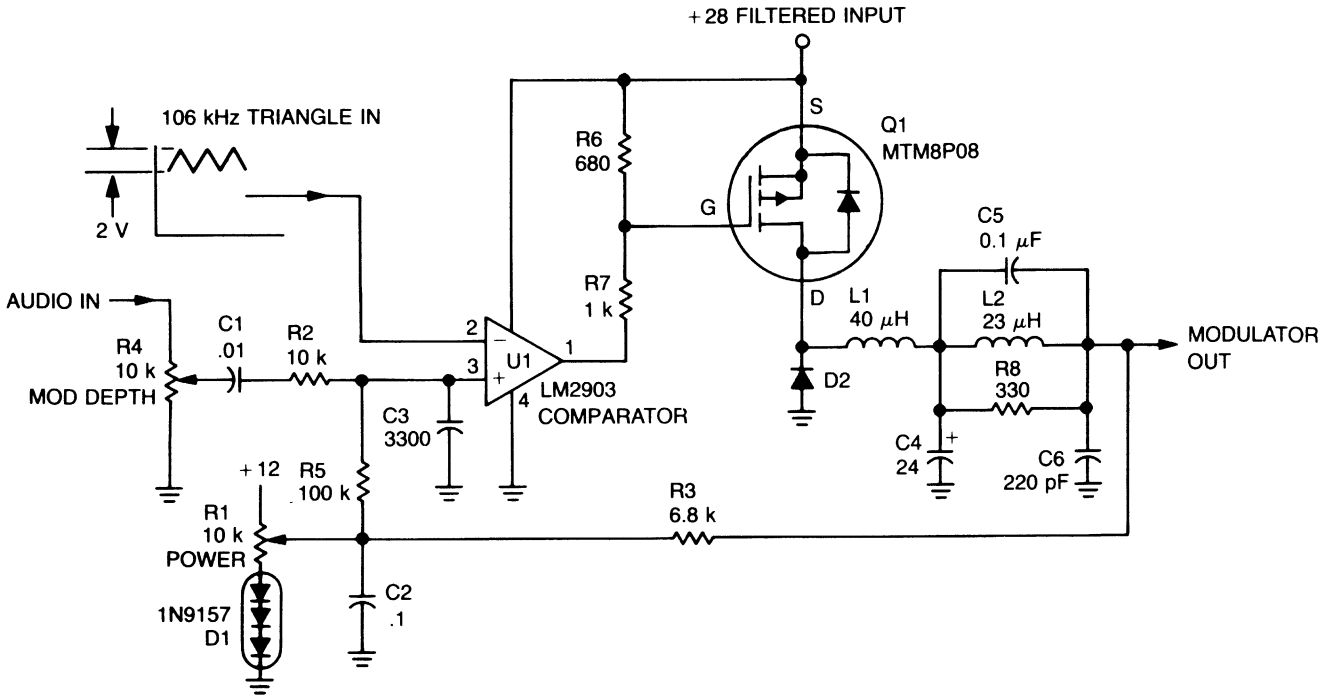
In the new circuit shown here, normal drain voltage is set at 12 V and is modulated from (ideally) 0 to 24 V for 100% amplitude modulation. Modulator requirements are approximately 5 A at the 12 V carrier level, rising to 10 A at modulation peaks of 24 V.

A single MTP8P10 performs the main switching function. With storage time eliminated from the switch, distortion caused by the modulator is eliminated and the predominant distortion of the transmitter is set by the modulated Class C stages. Furthermore, overall efficiency is improved by faster switching frequencies.

In operation, a 106 kHz triangular wave with a peak-to-peak amplitude of Vp is applied to the LM2903 comparator (U1). For any portion of the cycle in which Vp is greater than the reference input (pin 3 of U1), Q1 drain becomes 28 V minus the voltage drop due to R_{ds}. Thus, the output at the Q1 drain = $28(1 - E_{REF}/V_p)$, where E_{REF} is the reference voltage.

The variable cycle square wave output from the drain is applied to the low pass filter formed by L1, C4 and C6. This provides a near dc output with the L2-C5 resonant trap filtering the fundamental switching frequency. Diode D2 permits current in the low pass filter when Q1 is in OFF (energy stored in L1 and L2 is released).

E_{REF}, is derived from three sources. First, the dc level set by R4. Second, the 300-3000 Hz modulating frequency that shifts the reference at the modulating rate. Third, the dc feedback primarily controlled by R5. Capacitor C3 determines the closed loop cutoff frequency; it was chosen to compensate for the large phase shift introduced by the low pass filter.

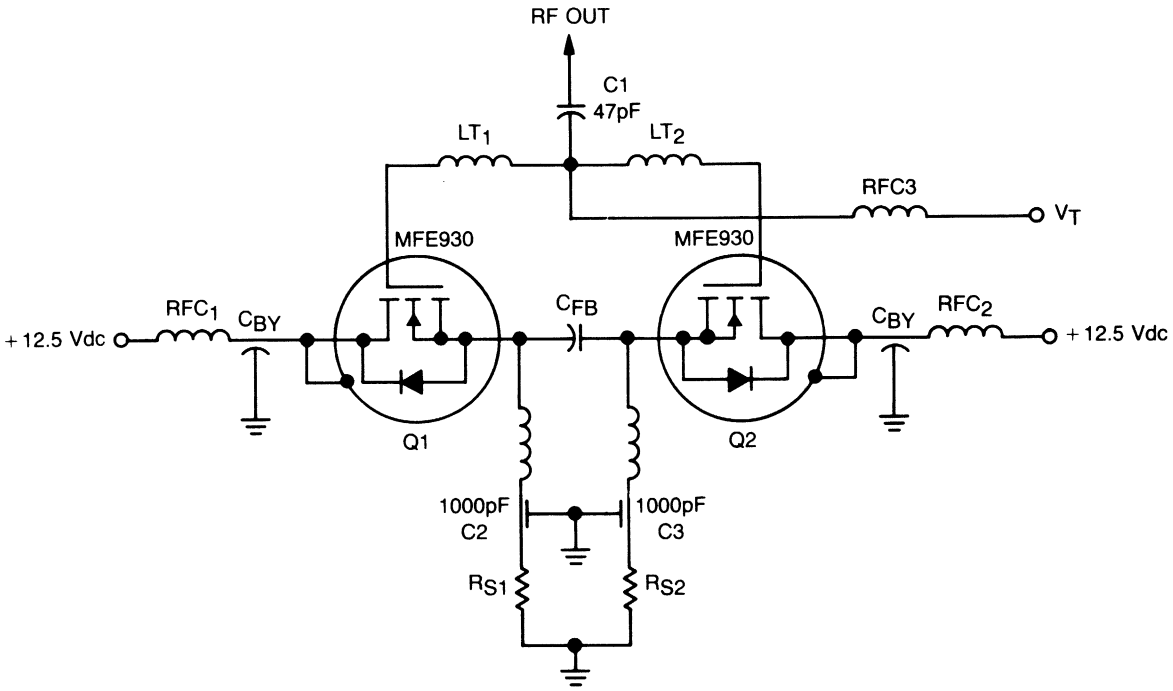


Balanced TMOS VCO

John Jones, *Dayton, OH*

This TMOS VCO operates in push-pull to produce 4 W at 70 MHz. It consists of two MFE930 TMOS devices in a balanced VCO that generally provides better linearity than that of single-ended types. Varactors are not used because the design takes advantage of the large change in "Miller" capacitance, C_{rss}, that is available in TMOS gate structures.

In the balanced VCO, the fundamental (f_o) and/or twice the fundamental ($2f_o$) can be coupled from the circuit at separate nodes. This makes the balanced oscillator very useful in phase-locked loops. The fundamental, $f_o = \frac{1}{2\pi}(L_t \cdot C_{rss})^{-1/2}$, where $L_t \approx 0.68\ \mu H$.



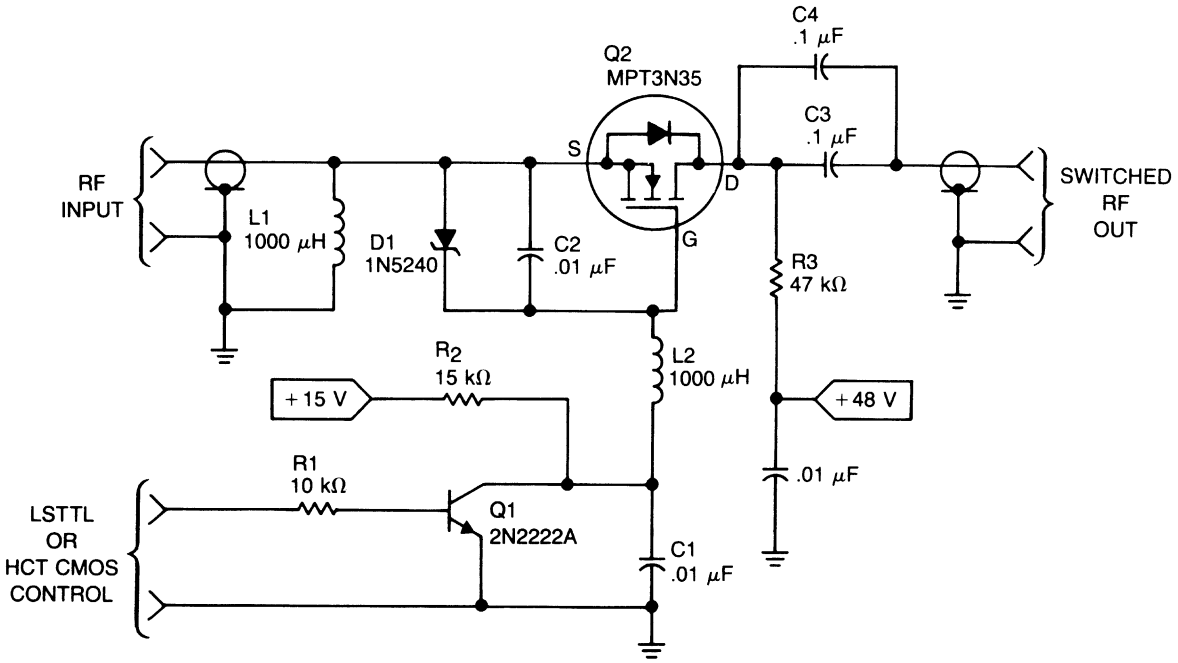
RF Power Switch

Robert Rouquette, *Harahan, LA*

PIN diodes have served well in RF power switching applications, but a TMOS Power FET provides acceptable performance with simpler drive requirements. The TMOS version lowers the overall cost and space requirements, when power supplies are included in the analysis. The Power FET does not need a heat sink other than the pc board, in this application.

A low current, high voltage supply is common to both the PIN and Power FET designs. The supply reverse biases the PIN diodes or the Power FET intrinsic diode in the OFF state. In the On state, a PIN diode switch requires 150 mA forward bias from a +5 V supply. The Power FET requires 1 mA from a +15 V supply in the ON state.

This RF power switch operates at 1.7 MHz with a 50v source and load. Its ON loss is 0.2 dB and its OFF isolation is 30 dB. It provides 40 W PEP, 45 V_{peak} and 0.9 A_{peak}. The control input can come from CMOS, TTL, LS, etc. to turn ON Q1, which turns ON Q2, a TMOS MTP3N35.



μP-Controlled Servo Amplifier With TMOS-Darlington Output

Ned Dammeyer, *New Bremen, OH*

The following requirements were established for a pulse width modulated (PWM) motor drive servo amplifier:

1. 24 V battery operation
2. <5 mA standby current
3. Survive a locked-rotor
4. Survive a shorted output
5. All positioning requires an initial full-on (acceleration)
6. Position loop closed through the μP
7. All safety circuits in hardware to meet the speed requirements to shut down rather than process an interrupt

The output stage is an "H" bridge consisting of two TIP140T NPN Darlington emitter followers (Q2 and Q7) and two MTP3055A TMOS Power FETs (Q4 and Q5). Q1 and Q8 PNP pre-drivers act as direction switches to supply the necessary current to source Q2 and Q7. PNP drivers Q3 and Q6 provide low impedance sourcing to turn on Q4 and Q5.

Two inputs are required from the μP: a direction command determined by the polarity between the command and feedback signals, a speed pulse determined by the magnitude of the error signal. In addition, a third signal from the servo amplifier notifies the μP of an over-current fault.

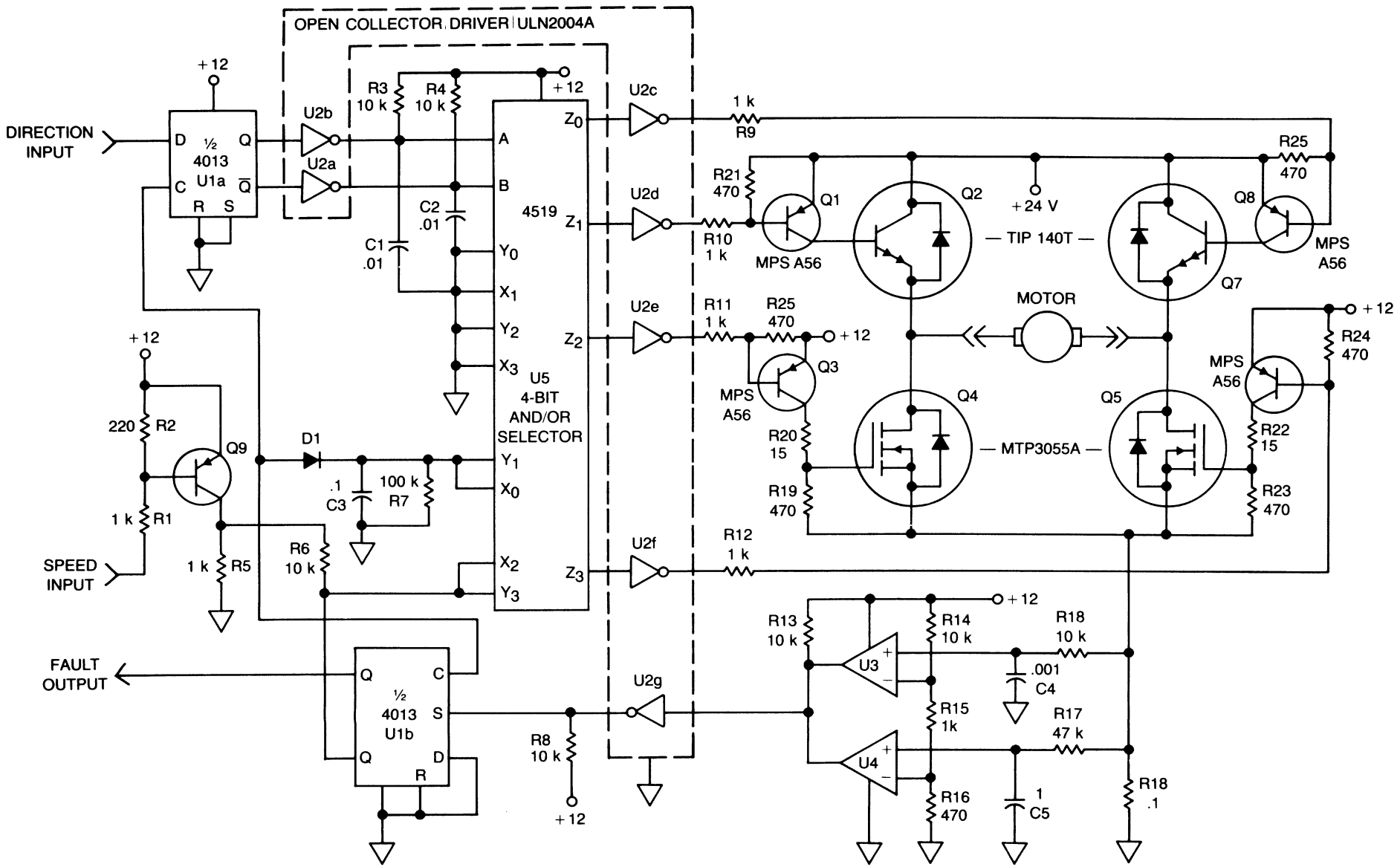
The position input is clocked into the U1a "D" latch on the leading edge of the first speed pulse following a direction change. Inputs A and B, applied to U5 (4-bit AND/OR Selector), select the inputs to be connected to the outputs. These inputs are derived from U1a via inverters U2a and U2b and R-C time constants consisting of R3-C1 and R4-C2. The time constants prohibit the possibility of both legs of the "H" bridge conducting simultaneously. This induces a lag on the initiation, or rising edge, of the direction that is selected.

Speed input is a 1 kHz, variable pulse width signal that is switched by driver transistor Q9 to inputs Y1, X0, X2 and Y3 of U5. If the direction input causes U5's A input to go high, all the "X" inputs to U5 are selected, and the following occurs:

1. Z0 output goes high, turning ON Q7
2. Z1 output goes low, disabling Q2
3. Z2 output is pulsed, driving Q4 at a variable pulse width
4. Z3 output goes low, disabling Q5

When this happens, the motor turns in the direction that nulls the position loop error. When there is no longer an error (no pulse width), the integrated inputs to U5's X0 and Y1 decay to zero, even though a direction is selected by U1a. If the B input to U5 is selected to go high, the opposite devices of the "H" bridge conduct and drive the motor in the opposite direction.

Comparator U4 provides current limiting in case of a locked rotor or over 20 msec acceleration time. Current limiting is also initiated if U3 catches the higher amplitude and fast transitions that occur if a system is miswired, or the output is shorted. In addition, a "Fault" signal is sent to U1b, which sends this information to the μP.

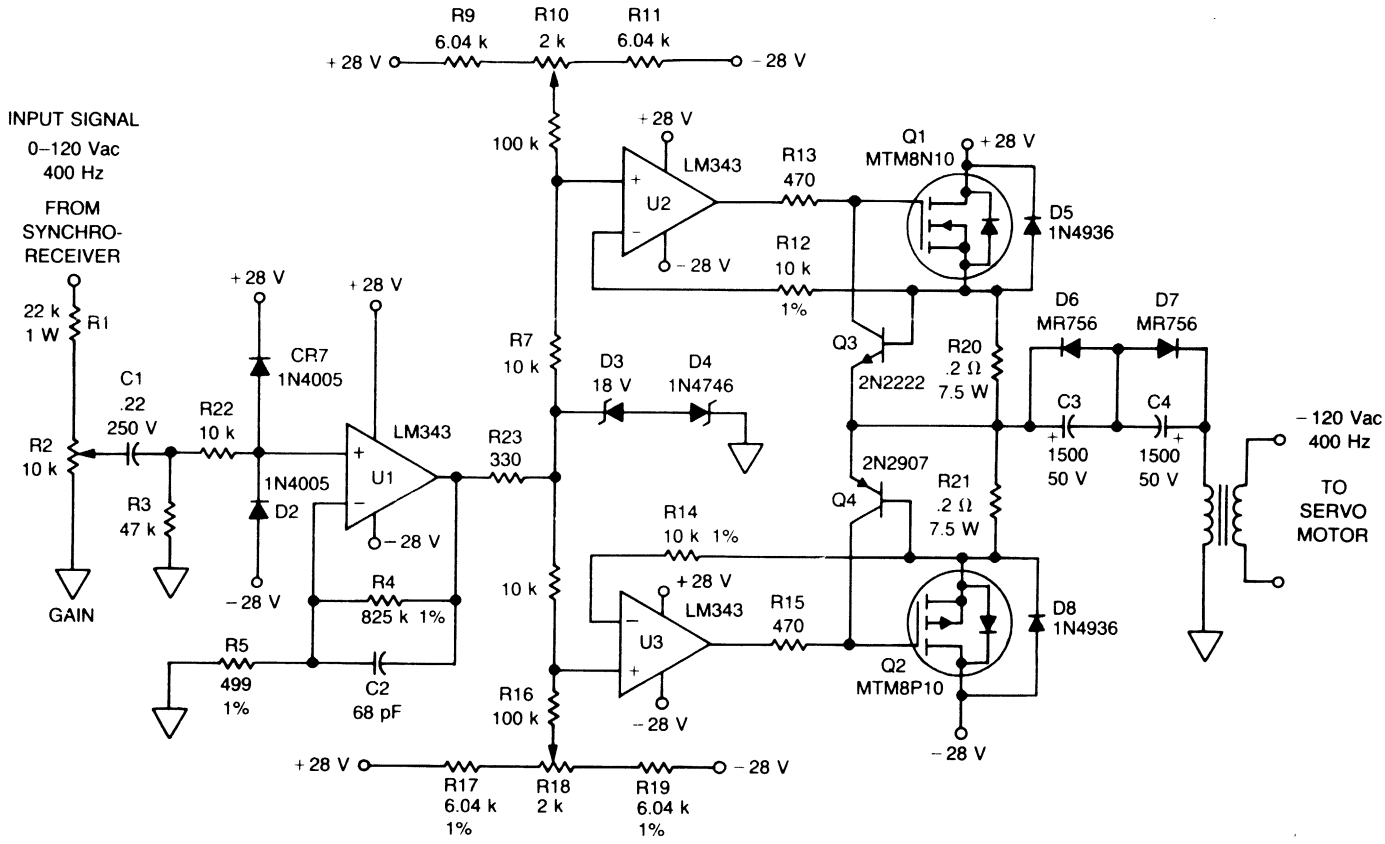

OPEN COLLECTOR DRIVER ULN2004A
DIRECTION INPUT
SPEED INPUT
FAULT OUTPUT
+12
+24 V
½ 4013 U1a
½ 4013 U1b
U2a
U2b
U2c
U2d
U2e
U2f
U2g
R1 1 k
R2 220
R3 10 k
R4 10 k
R5 1 k
R6 10 k
R7 100 k
R8 10 k
R9 1 k
R10 1 k
R11 1 k
R12 1 k
R13 10 k
R14 10 k
R15 1k
R16 470
R17 47 k
R18 .1
R19 470
R20 15
R21 470
R22 15
R23 470
R24 470
R25 470
C1 .01
C2 .01
C3 .1
C4 .001
C5 1
D1
Q1
Q2
Q3
Q4
Q5
Q7
Q8
Q9
MPS A56
TIP 140T
MTP3055A
MOTOR
U3
U4
U5 4-BIT AND/OR SELECTOR
4519

400-HZ Servo Amplifier

Larry Ducas, *Industry, CA*

In this 400-Hz servo amplifier, full advantage is taken of the low power drive requirements for TMOS devices. Operational amplifiers provide direct drive for the TMOS output Power FETs, which in turn drive the servo motor through a step-up transformer...no power driver circuits are needed. Another TMOS advantage is freedom from second breakdown, which can occur in bipolar devices.

The signal from a synchro receiver or a variable resistive cam follower (potentiometer) is boosted by operational amplifier U1, whose output swing is limited by back-to-back zeners D3 and D4. The signal is then applied to operational amplifiers U2 and U3, which drive the gates of Q1 and Q2, respectively. NPN transistor (Q3) is a fast current limiter for the N-channel MTM8N10; a PNP transistor (Q4) performs the same function for the P-channel MTM8P10. Capacitors C3 and C4 eliminate the need for accurate dc offset zeroing. T1 steps up the output voltage to 120 V for the 400 Hz servo motor.



Maximum Efficiency H Bridge Power Amplifier

Lealon R. McKenzie, *Tulsa, OK*

Today, many servo motor designs must meet international safety regulations, such as TUL/VDE shock hazards, which require secondary power supplies below 42.4 V. To meet these specifications and minimize current, the motor torque/voltage constants must be chosen for a maximum RPM load with the full secondary output of 40 V. Use of the full secondary output voltage dictates an "H" bridge power amplifier instead of a split secondary (±20 V) supply.

A number of "H" bridge configurations can be used, but the single side switching technique shown here has been found to be particularly effective. Referring to the figure, this bridge technique offers reduced C1 RMS and peak-to-peak current and the C1 effective series resistance (ESR) is removed from the L/R discharge path. Furthermore, switches Q2 and Q4 can be chosen with a lower ON resistance than Q1 and Q3, which improves efficiency twofold by increasing the percentage of time Q2 and Q4 conduct due to the L/R discharge time constant.

The next step is to choose the power switch. Fast switching speeds, large SOA, bidirectional current current carrying capacity, and the ability to select ON resistance as a function of cost makes TMOS the obvious and only choice. If the design operates just below the TUL/VDE safety extra low voltage (SELV) for maximum efficiency, use of P-channel FETs for Q1 and Q2 is required. P-channels are chosen because N-channel FETs need a gate voltage of 12 V with respect to the source in order to saturate. Therefore, to saturate and get a 40 V source voltage requires the gate voltage to be 40 + 12, or 52 V; that is over the SELV.

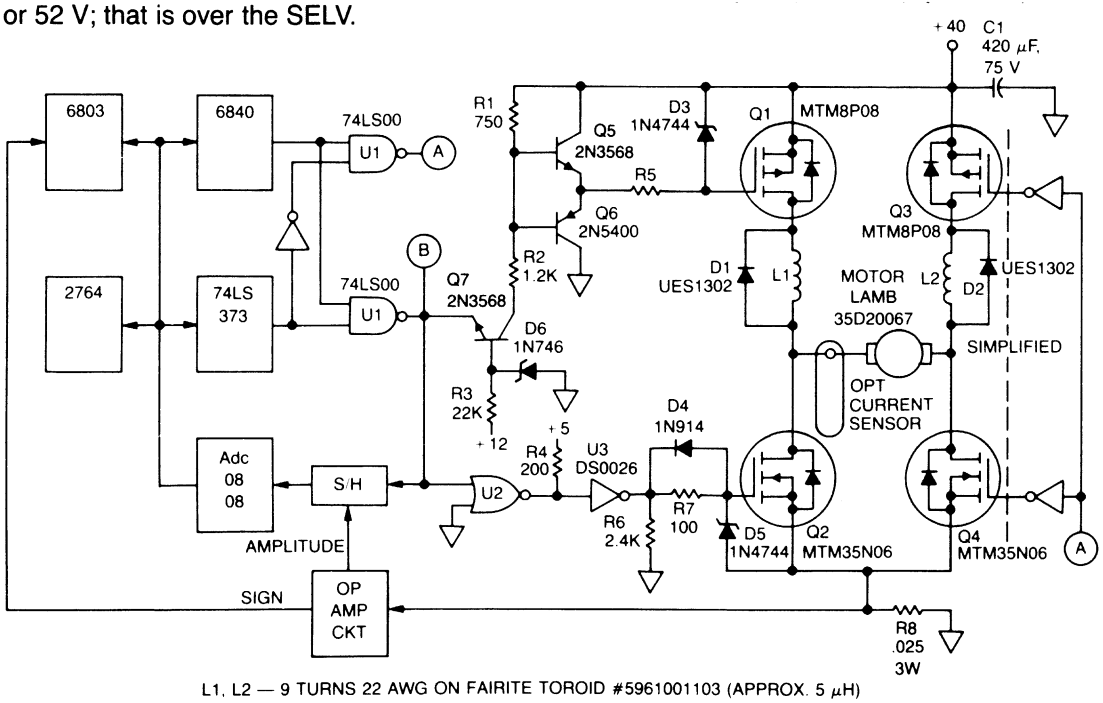
Specifications for the amplifier are:

C1 ESR	0.1
Q1 and Q3 $r_{DS(ON)}$	0.4
Q2 and Q4 $r_{DS(ON)}$	0.28
Motor resistance	0.5
Motor inductance	2.5 mH
Motor KT	54 oz-in./A
Motor load profile	540 oz-in. accelerated from 0 to 250 RPM
Servo control	Current-controlled minor loop

In the circuit shown, drive circuits for Q3 and Q4 are shown simplified; they originate at point A and are identical to the drive circuits that originate at point B and are applied to Q1 and Q2.

Based on the required motor current, the 6803 microprocessor generates a pulse width modulated signal and applies it to U1 via the 6840 timer. Direction information is produced by the 74LS373; if the direction is high, point A goes high and U1 pulses Q7 low. This causes Q7 to turn ON, dropping the base and emitter voltages of Q5 and Q6 from 40 to approximately 28 V. Q1's gate is -12 V with respect to its source, so it turns ON. At the same time, the low pulse from U1, amplified by U2 and U3, drops Q2's gate from +12 V to 0 V, turning Q2 OFF.

The motor inductance is charged by current from C1 through Q1, L1, Q4 and R8. L1 and L2 provide the switching current limit protection needed for synchronous rectification.



L1, L2 — 9 TURNS 22 AWG ON FAIRITE TOROID #5961001103 (APPROX. 5 μH)

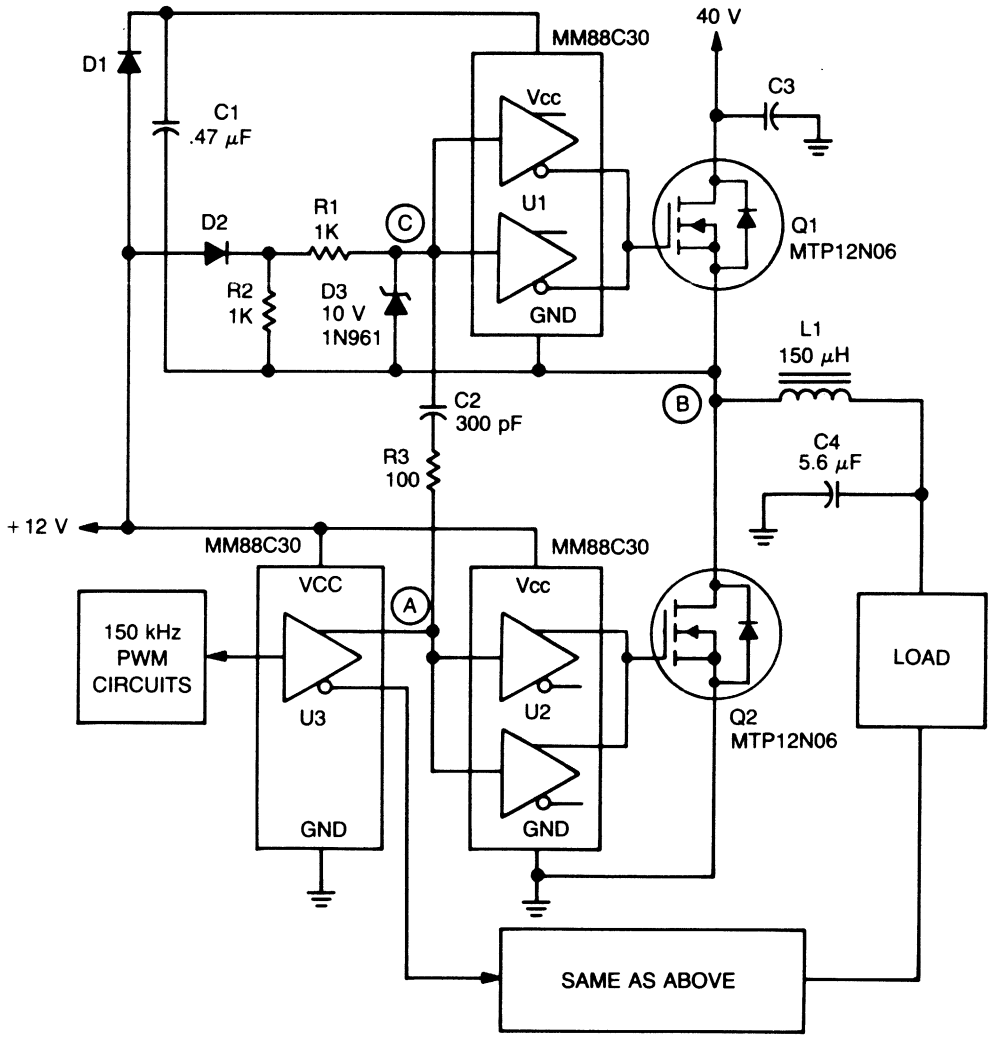
PWM Servo Amplifier

Darrel Russon, *Seattle, WA*

A major feature of this PWM servo amplifier is elimination of the need for a pulse transformer.

A 150 kHz pulse width modulated signal is applied to U3, with its complementary outputs applied to identical circuits to drive the load. When point A goes high, Q2 is ON and point B is at ground potential. The VCC for U1 is maintained through D1 and Q1 is held OFF by D2. When point A goes low, Q2 turns OFF, point C is pulled low by C2, which turns Q1 ON. The time constant of R1, R3 and C2 can maintain Q1 ON just long enough to allow the voltage at point B to start rising. As point B rises, it charges C2 by forward biasing D3, maintaining point C low with respect to U1 and keeping Q1 turned ON.

With point B at 40 V, D2 is OFF and point C is held low by R1 and R2, and VCC for U1 is maintained by the charge on C1. When point A goes high again, Q2 again turns ON, C2 pushes point C high and turns Q1 OFF long enough to allow the voltage at point B to start falling. C2 is now discharged by reverse-biased D3, which keeps point C high with respect to U1 and keeps Q1 OFF. Once point B reaches ground potential, D1 again turns ON, recharging C1 and maintaining VCC for U1. D2 also turns ON and keeps Q1 OFF.



DC Servo Drive Employs Bipolar Control Input

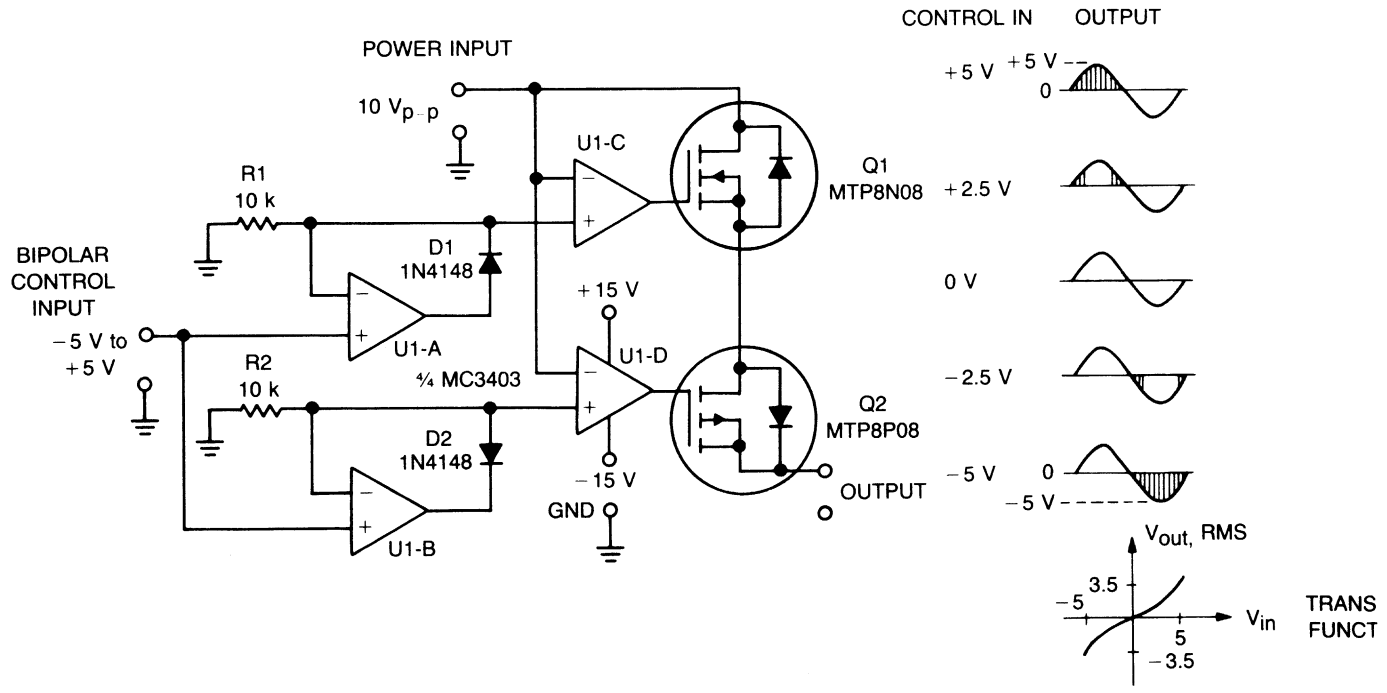
Davide Andrea, *Boulder, CO*

This circuit accepts bipolar control inputs of ±5 V and provides a phase-chopped output to a dc load (such as a servo motor) of the same polarity as the input. The RMS voltage of the output is closely proportional to the control input voltage.

N-channel and P-channel TMOS devices, Q1 and Q2, are connected in anti-series to form a bidirectional switch through which current can flow in either the forward or reverse direction. Control circuits turn Q1 and Q2 ON when they are reverse biased, bypassing their reverse rectifier and increasing circuit efficiency. Each device is allowed to turn OFF only when forward biased.

The Q1-Q2 switch connects the ac power source to the load when its instantaneous voltage is the same polarity and less than the control voltage. U1a is configured as an ideal positive rectifier whose output follows the control voltage when it is positive, and is zero otherwise. Similarly, U1b is a negative rectifier. U1c turns Q1 ON whenever the ac input voltage is lower than the positive rectifier output. For negative control voltages, Q1 is turned ON only during the negative half-cycle. For positive control voltages, Q1 is turned ON during the end portions of the positive half-cycle. Similarly, U1d turns Q2 ON whenever the ac input voltage is higher than the output of the negative rectifier.

Operating voltages were selected to drive the TMOS devices for best conductance and to avoid exceeding the maximum TMOS gate voltage ratings and the operational amplifier supply. With the selection of a few components, operation at the maximum drain-source voltage is possible.



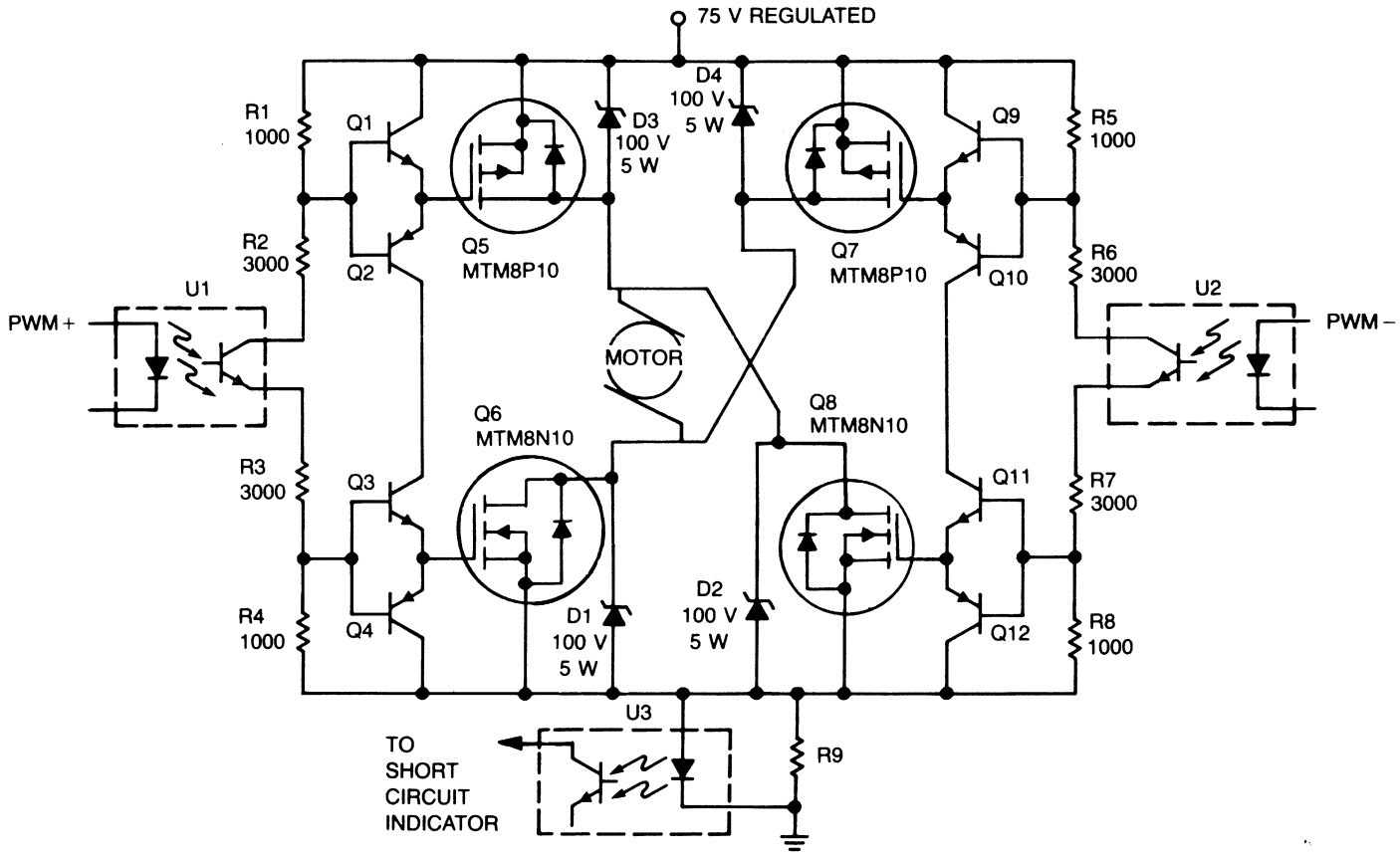
Servo Motor Drive Amplifier

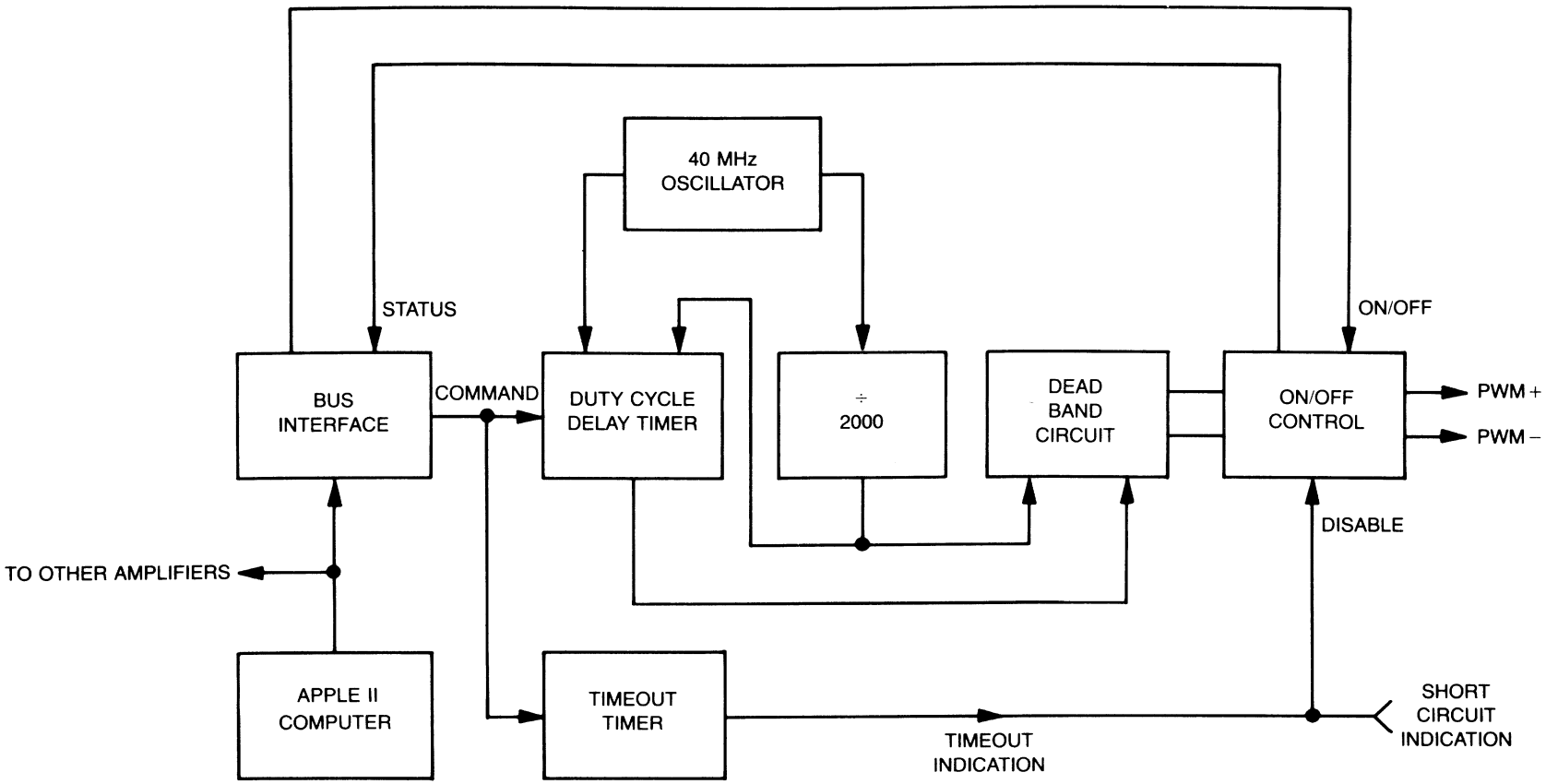
S.M. Killough, *Oak Ridge, TN*

Digital ICs and opto-isolators provide the drive for this TMOS servo amplifier, resulting in fewer analog circuits and less drift. Fast and consistent turn-on and turn-off characteristics also enable accurate analog output results directly from the digital signal without the need for analog feedback.

The resulting 12-bit resolution amplifier, designed for Apple II™ systems, can be chained with up to eight more amplifiers and still only require connection to one Apple II card slot. The mostly digital amplifier is easy to build and troubleshoot, resulting in a more economical, simpler and reliable high performance amplifier.

An "H" bridge configuration is employed for the servo amplifier, which obtains complementary PWM inputs from digital control circuits. The PWM inputs are applied via opto-isolators, which keep the digital control logic isolated from the 75 V supply used for the amplifier. A short circuit indicator is provided by opto-isolator U3; if there is a short, the drop across R9 increases to a value sufficient to activate the isolator and send a short indication to the digital control logic.



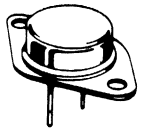

40 MHz
OSCILLATOR
STATUS
ON/OFF
BUS
INTERFACE
COMMAND
DUTY CYCLE
DELAY TIMER
÷
2000
DEAD
BAND
CIRCUIT
ON/OFF
CONTROL
PWM +
PWM –
DISABLE
TO OTHER AMPLIFIERS
APPLE II
COMPUTER
TIMEOUT
TIMER
TIMEOUT
INDICATION
SHORT
CIRCUIT
INDICATION

Selection by Package

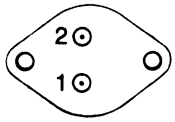
Tables 1 through 16 are shown by package type. Within the tables the devices are arranged by breakdown voltage and on-resistance as the primary selection criteria.

TMOS Power MOSFETs

Metal Packages — TO-204



TO-204 (Formerly TO-3)



CASE 1-04 and CASE 1-05

Table 1 — P-Channel

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
500	6	1	MTM2P50	2	75
450			MTM2P45		
250	4	1.5	MTM3P25	3	
	3	2.5	MTM5P25	5	
	2	4	MTM8P25	8	
200	1	2.5	MTM5P20	5	
	0.7	4	MTM8P20	8	125
180	1	2.5	MTM5P18	5	75
	0.7	4	MTM8P18	8	125
100	0.4		MTM8P10		75
	0.3	6	MTM12P10	12	
	0.15	10	MTM20P10	20	125
80	0.4	4	MTM8P08	8	75
	0.3	6	MTM12P08	12	
	0.15	10	MTM20P08	20	125
60	0.6	3.5	MTM7P06	7	75
	0.3	6	MTM12P06	12	
	0.2	10	MTM20P06	20	100
50	0.6	3.5	MTM7P05	7	75
	0.3	6	MTM12P05	12	
	0.2	10	MTM20P05	20	100

* @ 25°C

Table 2 — N-Channel

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
1000	10	0.5	MTM1N100	1	75
	7	1.5	MTM3N100	3	125
	3	2.5	MTM5N100	5	150
950	10	0.5	MTM1N95	1	75
	7	1.5	MTM3N95	3	125
	3	2.5	MTM5N95	5	150
900	8	1	MTM2N90	2	75
	5	2	MTM4N90	4	125
	3	3	MTM6N90	6	150
850	8	1	MTM2N85	2	75
	5	2	MTM4N85	4	125
	3	3	MTM6N85	6	150
800	7	1.5	MTM3N80	3	75
	2	3	BUZ84	5.3	125
	1.5		BUZ84A	6	
750	7	1.5	MTM3N75	3	75
600	6	1	MTM2N60	2	
	2.8	3	2N6823	3	
	2.5	1.5	MTM3N60		
	1.6	6	2N6826	6	150
	1.2	3	MTM6N60		

* @ 25°C

Table 2 — N-Channel — continued

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
600	0.5	4	MTM8N60	8	150
550	6	1	MTM2N55	2	75
	2.5	1.5	MTM3N55	3	
	1.2	3	MTM6N55	6	150
	0.5	4	MTM8N55	8	
500	4	1	MTM2N50	2	75
			IRF422		40
	3		IRF420	2.5	
		1.5	MTM3N50	3	75
	2	2.5	IRF432	4	
	1.5		IRF430	4.5	
		2	MTM4N50	4	
		3	2N6762	4.5	
	1.1	4	IRF442	7	125
	0.85		IRF440	8	
	0.8	3.5	MTM7N50	7	150
	0.5	7	IRF452	12	
	0.4		IRF450	13	
		7.75	2N6770**	12	
		7.5	MTM15N50	15	250
450	4	1	MTM2N45	2	75
			IRF423		40
	3		IRF421	2.5	
		1.5	MTM3N45	3	75
	2	2.5	IRF433	4	
			2N6761		
	1.5		IRF431	4.5	
		2	MTM4N45	4	
	1.1	4	IRF443	7	125
	0.85		IRF441	8	
	0.8	3.5	MTM7N45	7	150
	0.5	7	IRF453	12	
			2N6769	11	
	0.4		IRF451	13	
		7.5	MTM15N45	15	250
400	3.3	1.5	MTM3N40	3	75
	2.5		IRF322	2.5	40
	1.8		IRF320	3	
		2	MTM4N40	4	75
	1.5	3	IRF332	4.5	
	1		IRF330	5.5	
		2.5	MTM5N40	5	

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
400	1	3.5	2N6760**	5.5	75
	0.8	5	IRF342	8	125
	0.55		IRF340	10	
		4	MTM8N40	8	150
	0.4	8	IRF352	13	
	0.3		IRF350	15	
		9	2N6768	14	
		7.5	MTM15N40	15	250
350	3.3	1.5	MTM3N35	3	75
	2.5		IRF323	2.5	40
	1.8		IRF321	3	
		2	MTM4N35	4	75
	1.5	3	IRF333	4.5	
			2N6759		
	1		IRF331	5.5	
		2.5	MTM5N35	5	
	0.8	5	IRF343	8	125
	0.55		IRF341	10	
	5	4	MTM8N35	8	150
	0.4	8	IRF353	13	
		7.75	2N6767	12	
	0.3	8	IRF351	15	
		7.5	MTM15N35		250
250	0.45	5	MTM10N25	10	100
200	1.2	2.5	IRF222	4	40
	1		MTM5N20	5	75
	0.8		IRF220		40
	0.7	3.5	MTM7N20	7	75
	0.6	5	IRF232	8	
	0.4		IRF230	9	
			2N6758		
		4	MTM8N20	8	
	0.35	6	MTM12N20	12	100
	0.22	10	IRF242	16	125
	0.18		IRF240	18	
	0.16	7.5	MTM15N20	15	150
	0.12	16	IRF252	25	
	0.085		IRF250	30	
		19	2N6766		
	0.08	20	MTM40N20	40	250
180	1	2.5	MTM5N18	5	75
	0.7	3.5	MTM7N18	7	

* @ 25°C

**Available at JAN, JTX, JTXV levels

TMOS™

Table 2 — N-Channel — continued

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
180	0.4	4	MTM8N18	8	75
	0.35	6	MTM12N18	12	100
	0.16	7.5	MTM15N18	15	150
	0.08	20	MTM40N18	40	250
150	1.2	2.5	IRF223	4	40
	0.8		IRF221	5	
	0.7	3.5	MTM7N15	7	75
	0.6	5	2N6757	8	
			IRF233		
	0.5	4	MTM8N15		
	0.4	5	IRF231	9	
	0.3		MTM10N15	10	
	0.25	7.5	MTM15N15	15	150
	0.22	10	IRF243	16	125
	0.18	16	IRF241	18	
	0.12	10	MTM20N15	20	150
		16	IRF253	25	
			2N6767		
	0.085		IRF251	30	
	0.06	22.5	MTM45N15	45	250
120	0.7	3.5	MTM7N12	7	75
	0.5	4	MTM8N12	8	
	0.3	5	MTM10N12	10	
	0.25	7.5	MTM15N12	15	150
	0.12	10	MTM20N12	20	
	0.06	22.5	MTM45N12	45	250
100	0.5	4	MTM8N10	8	75
	0.4		IRF122	7	40
	0.33	5	MTM10N10	10	75
	0.3		IRF120	8	40
	0.25	8	IRF132	12	75
	0.18		IRF130	14	
		6	MTM12N10	12	
		9	2N6756	14	
	0.15	10	MTM20N10	20	100
	0.11	15	IRF142	24	125
	0.085		IRF140	27	

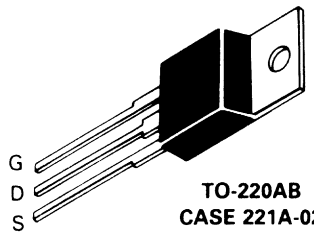
* @ 25°C

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
100	0.08	20	IRF152	33	150
	0.07	12.5	MTM25N10	25	
	0.055	20	IRF150	40	
		24	2N6764**	38	
	0.04	27.5	MTM55N10	55	250
80	0.5	4	MTM8N08	8	75
	0.33	5	MTM10N08	10	
	0.18		MTM12N08	12	
	0.15	10	MTM20N08	20	100
	0.07	12.5	MTM25N08	25	150
	0.04	27.5	MTM55N08	55	250
60	0.4	4	IRF123	7	40
	0.3		IRF121	8	
	0.25	8	IRF133	12	75
			2N6755		
		5	MTM10N06	10	
	0.2	6	MTM12N06	12	
	0.18	8	IRF131	14	
	0.16	7.5	MTM15N06	15	
	0.15		MTM15N06L		
	0.11	15	IRF143	24	125
	0.1	12.5	MTM25N06L	25	100
	0.085	15	IRF141	27	125
	0.08	12.5	MTM25N06	25	100
		20	IRF153	33	150
			2N6763	31	
	0.055	17.5	MTM35N06	35	
		20	IRF151	40	
	0.028	30	MTM60N06	60	250
50	0.25	5	MTM10N05	10	75
	0.2	6	MTM12N05	12	
	0.16	7.5	MTM15N05	15	
	0.15		MTM15N05L		
	0.1	12.5	MTM25N05L	25	100
	0.08	12.5	MTM25N05L		
	0.055	17.5	MTM35N05	35	150
	0.028	30	MTM60N05	60	250

**Available at JAN, JTX, JTXV levels

TMOS Power MOSFETs

Plastic Packages



TO-220AB
CASE 221A-02

Table 3 — P-Channel

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
500	6	1	MTP2P50	2	75
450			MTP2P45		
250	4	1.5	MTP3P25	3	
	3	2.5	MTP5P25	5	
	2	4	MTP8P25	8	
200	1	2.5	MTP5P20	5	
180			MTP5P18		
100	0.4	4	MTP8P10	8	
100	0.3	6	MTP12P10	12	75
80	0.4	4	MTP8P08	8	
	0.3	6	MTP12P08	12	
60	0.6	3.5	MTP7P06	7	
	0.3	6	MTP12P06	12	
	0.2	10	MTP20P06	20	100
50	0.6	3.5	MTP7P05	7	75
	0.3	6	MTP12P05	12	

* @ 25°C

Table 4 — N-Channel

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
1000	10	0.5	MTP1N100	1	75
	7	1.5	MTP3N100	3	
950	10	0.5	MTP1N95	1	
	7	1.5	MTP3N95	3	
900	8	1	MTP2N90	2	
	5	2	MTP4N90	4	
850	8	1	MTP2N85	2	
	5	2	MTP4N85	4	
800	7	1.5	MTP3N80	3	
750			MTP3N75		
600	12	0.5	MTP1N60	1	
	6	1	MTP2N60	2	
	2.5	1.5	MTP3N60	3	
	1.2	3	MTP6N60	6	125
550	12	0.5	MTP1N55	1	75
	6	1	MTP2N55	2	
	2.5	1.5	MTP3N55	3	
	1.2	3	MTP6N55	6	125
500	8	0.5	MTP1N50	1	50
	4	1	MTP2N50	2	75
			IRF822		40
500	3	1.5	IRF820	2.5	40
			MTP3N50	3	75
	2		IRF832	4	
	1.5		IRF830	4.5	
			MTP4N50	4	
	1.1	4	IRF842	7	125
	0.85		IRF840	8	
	0.8		MTP8N50		
450	8	0.5	MTP1N45	1	50
	4	1	MTP2N45	2	75
			IRF823		40
	3		IRF821	2.5	
		1.5	MTP3N45	3	75
	2	2.5	IRF833	4	
	1.5	2	MTP4N45		
		2.5	IRF831	4.5	
	1.1	4	IRF843	7	125
	0.85		IRF841	8	
	0.8		MTP8N45		
400	5	0.8	IRF712	1.3	20
		1	MTP2N40	2	50
	3.6	0.8	IRF710	1.5	20

* @ 25°C

TMOS™

Table 4 — N-Channel — continued

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
400	3.3	1.5	MTP3N40	3	75
	2.5		IRF722	2.5	40
	1.8		IRF720	3	
		2	MTP4N40	4	75
	1.5	3	IRF732	4.5	
	1		IRF730		
		2.5	MTP5N35	5	
	0.8	5	IRF742	8	125
	0.55		IRF740	10	
			MTP10N40		
350	5	1	MTP2N35	2	50
		0.8	IRF713	1.3	20
	3.6		IRF711	1.5	
	3.3	1.5	MTP3N35	3	75
	2.5		IRF723	2.5	40
	1.8		IRF721	3	
		2	MTP4N35	4	75
	1.5	3	IRF733	4.5	
	1		IRF731	5.5	
		2.5	MTP5N35	5	
	0.8	5	IRF743	8	125
	0.55		IRF741	10	
			MTP10N35		
250	2	1	MTP2N25	2	50
	0.45	5	MTP10N25	10	100
200	2.4	1.25	IRF612	2	20
	1.8	1	MTP2N20		50
	1.5	1.25	IRF610	2.5	20
	1.2	2	MTP4N20	4	50
		2.5	IRF622		40
	1		MTP5N20	5	75
	0.8		IRF620		40
	0.7	3.5	MTP7N20	7	75
	0.6	5	IRF632	8	
	0.4		IRF630	9	
		4	MTP8N20	8	
	0.35	6	MTP12N20	12	100
200	0.22	10	IRF642	16	125
	0.18		IRF640	18	
180	1.8	1	MTP2N18	2	50
	1.2	2	MTP4N18	4	
	1	2.5	MTP5N18	5	75
	0.7	3.5	MTP7N18	7	
	0.4	4	MTP8N18	8	
	0.35	6	MTP12N18	12	100
150	2.4	1.25	IRF613	2	20
	1.5		IRF611	2.5	
	1.3	1.5	MTP3N15	3	50
	1.2	2.5	IRF623	4	40
	0.9		MTP5N15	5	50
	0.8		IRF621	4	40
	0.7	3.5	MTP7N15	7	75
	0.6	5	IRF633	8	
	0.5	4	MTP8N15		
	0.4	5	IRF631	9	
	0.3		MTP10N15	10	
	0.25	7.5	MTP15N15	15	100
	0.22	10	IRF643	16	125
	0.18		IRF641	18	
120	1.3	1.5	MTP3N12	3	50
	0.9	2.5	MTP5N12	5	
	0.7	3.5	MTP7N12	7	75
	0.5	4	MTP8N12	8	
	0.3	5	MTP10N12	10	
	0.25	7.5	MTP15N12	15	100
100	0.8	2	MTP4N10	4	50
		3	MTP6N10	6	
		2	IRF512	3.5	20
	0.6		IRF510	4	
	0.5	4	MTP8N10	8	75
	0.4		IRF522	7	40
	0.33	5	MTP10N10	10	75
	0.3	4	IRF520	8	40
	0.25	8	IRF532	12	75

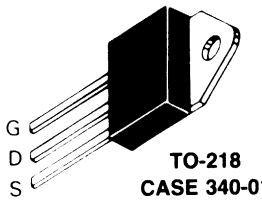
* @ 25°C

Table 4 — N-Channel — continued

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
100	0.25	5	MTP10N10M	10	75
	0.18	8	IRF530	14	
		6	MTP12N10	12	
	0.15	10	MTP20N10	20	100
	0.11	15	IRF542	24	125
	0.085		IRF540	27	
		12.5	MTP25N10	25	
80	0.8	2	MTP4N08	4	50
		3	MTP6N08	6	
	0.5	4	MTP8N08	8	75
	0.33	5	MTP10N08	10	
	0.18	6	MTP12N08	12	
	0.15	10	MTP20N08	20	100
	0.085	12.6	MTP25N08	25	125
60	0.8	2	IRF513	3.5	20
	0.6		IRF511	4	
		2.5	MTP5N06	5	50
	0.4	3.5	MTP7N06	7	
		4	IRF523		40
	0.3		IRF521	8	
	0.28	5	MTP10N06	10	75
	0.25	8	IRF533	12	
60	0.2	6	MTP12N06	12	75
	0.18	8	IRF531	14	
	0.16	7.5	MTP15N06	15	
	0.15		MTP15N06L		
		6	MTP3055A	12	40
	0.11	15	IRF543	24	125
	0.085		IRF541	27	
	0.08	12.5	MTP25N06	25	100
50	0.6	2.5	MTP5N05	5	50
	0.4	3.5	MTP7N05	7	
	0.28	5	MTP10N05	10	75
	0.16	7.5	MTP15N05	15	
	0.15		MTP15N05L		
	0.12	6	BUZ71A	12	40
	0.1		BUZ71		
		10	BUZ10	19	75
		7	MTP14N05A	14	40
	0.08	8	MTP16N05A	16	
		12.5	MTP25N05	25	100
	0.06	15	BUZ11A		75
	0.04		BUZ11	30	

* @ 25°C

Plastic Packages — TO-218



TO-218
CASE 340-01

TMOS™

Table 5 — P-Channel

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
200	0.7	4	MTH8P20	8	125
180			MTH8P18		
100	0.15	10	MTH20P10	20	
80	0.15	10	MTH20P08	20	125
60	0.14	12.5	MTH25P06	25	
50			MTH25P05		

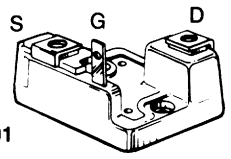
* @ 25°C

Table 6 — N-Channel

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
1000	3	2.5	MTH5N100	5	150
950			MTH5N95		
900		3	MTH6N90	6	
850			MTH6N85		
600	1.2		MTH6N60		
	0.5	4	MTH8N60	8	
550	1.2	3	MTH6N55	6	
	0.5	4	MTH8N55	8	
500	0.8	3.5	MTH7N50	7	
	0.4	7	MTH13N50	13	
450	0.8	3.5	MTH7N45	7	
	0.4	7	MTH13N45	13	
400	0.55	4	MTH8N40	8	
	0.3	7.5	MTH15N40	15	
350	0.55	4	MTH8N35	8	
	0.3	7.5	MTH15N35	15	
200	0.16	7.5	MTH15N20	15	150
	0.08	15	MTH30N20	30	
180	0.16	7.5	MTH15N18	15	
	0.08	15	MTH30N18	30	
150	0.12	10	MTH20N15	20	
	0.06	17.5	MTH35N15	35	
120	0.12	10	MTH20N12	20	
	0.06	17.5	MTH35N12	35	
100	0.07	12.5	MTH25N10	25	
	0.04	20	MTH40N10	40	
80	0.07	12.5	MTH25N08	25	
	0.04	20	MTH40N08	40	125
60	0.055	17.5	MTH35N06	35	150
	0.028	20	MTH40N06	40	
50	0.055	17.5	MTH35N05	35	
	0.028	20	MTH40N05	40	

* @ 25°C

Energy Management Series



P_D = 250 W

CASE 353-01

Mounting base is connected to the drain.

Table 7 — N-Channel (Case 353-01)

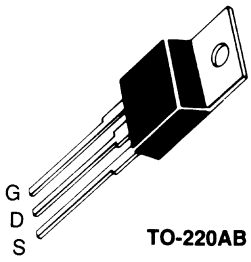
$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) (Amps) Max		Device	I_D (Amps) Max	P_D* (Watts) Max
600	0.25	10	MTE20N60	20	250
550			MTE20N55		
500	0.2	12.5	MTE25N50	25	
450			MTE25N45		
400	0.15	15	MTE30N40	30	
350			MTE30N35		
200	0.048	30	MTE60N20	60	
180	0.048	30	MTE60N18	60	250
150	0.038	32.5	MTE65N15	65	
120			MTE65N12		
100	0.028	37.5	MTE75N10	75	
80			MTE75N08		
60	0.018	50	MTE100N06	100	
50			MTE100N05		

* @ 25°C

Gain Enhanced MOSFETs (GEMFETs)

This relatively new series of power field-effect transistors combines the high input resistance of a MOSFET with the low internal on-resistance of a bipolar transistor to provide more efficient performance than either a MOSFET or bipolar device in low-frequency switching service. Recommended for motor drive circuits, home appliances, and other applications where high switching speed is not a requirement. All are N-Channel.

TO-204AA
(TO-3)



TO-220AB

Table 8 — TO-204AA

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) (Amps) Max		Device	I_D (Amps) Max	P_D* (Watts) Max
500	0.27	10	MGM20N50	20	100
	1.6	2.5	MGM5N50	5	50
450	0.27	10	MGM20N45	20	100
	1.6	2.5	MGM5N45	5	50

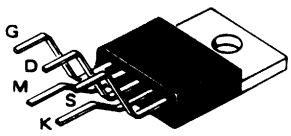
* @ 25°C

Table 9 — TO-220AB

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) (Amps) Max		Device	I_D (Amps) Max	P_D* (Watts) Max
500	0.27	10	MGP20N50	20	100
	1.6	2.5	MGP5N50	5	50
450	0.27	10	MGP20N45	20	100
	1.6	2.5	MGP5N45	5	50

* @ 25°C

TMOS SENSEFETs™



CASE 314B
(5 PIN TO-220)

SENSEFETs are conventional power MOSFETs with an option provided to sense the drain current by measuring a small proportion of the total drain current. These devices are ideal for current mode switching regulators and motor controls.

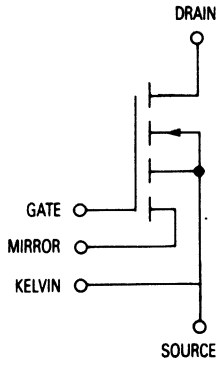


Table 10 — Case 314B

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
60	0.05	12.5	MTP25N06M	25	100
80	0.07		MTP25N08LM		
100	0.5	5	MTP10N10M**	10	75
250	4		MTP10N25M		100
450		1	MTP2N45M	2	50
	1.2	2.5	MTP5N45M	5	100

Device with LM suffix is low threshold device that turns fully on with 5 volts of drive between gate and source. All others require 10 volt drive.

* @ 25°C

** Indicates available from stock, others are planned for introduction.

DPAK

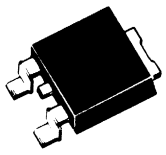
Table 11 — Case 369A-02 Surface Mount
Case 369-02 Insertion Mountable**

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (Amps) Max	P_D* (Watts) Max
200	0.7	2	MTD4N20	4	20
180			MTD4N18		
150	0.3	3	MTD6N15	6	
120			MTD6N12		
60	0.6	2	MTD4P06†	4	
	0.4	2.5	MTD5N06	5	
	0.15	4	MTD3055A	8	
50	0.6	2	MTD4P05†	4	
	0.4	2.5	MTD5N05	5	
	0.1	5	MTD10N05A	10	

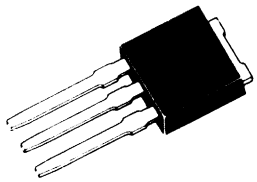
* @ 25°C

** Add -1 to part number to order insertion mountable package

† Indicates P-Channel

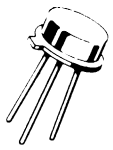


CASE 369A-02



CASE 369-02

Small-Signal MOSFETs



TO-205AF Type
(TO-39)

Table 12 — Switches and Choppers — TO-205AF

$V_{(DSS)}$ (Volts)	$r_{DS(on)}$ @ I_D (Ohms)	(Amps)	Device	$I_{D(Cont)}$ (Amps)	P_D @ T_C = 25°C (Watts)
240	6	0.5	VN2406B	0.63	2.5
	10	0.5	VN2410B	0.63	2.5
200	0.8	2.25	2N6790	3.5	20
	0.8	2	IRFF220	3.5	20
	1.5	1.5	2N6784	2.25	15
	6.4	0.25	MFE9200	0.4	1.8
170	6	0.5	VN1706B	0.63	2.5
	10	0.5	VN1710B	0.63	2.5
150	12	0.1	MFE4150	0.250	6.25
100	0.3	3	IRFF120	6	20
90	4	1	2N6661	0.9	6.25
60	3	1	2N6660	1.1	6.25
	5	0.5	MFE910	1	6.25
35	1.8	1	2N6659	1.4	6.25
30	1.2	1	VN0300B	1.25	6.25
	2.5	1	VP0300P	1.25	6.25

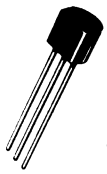
Table 13 — 4 Pin Dip — Case 370-01

CASE 370-01

P_D @ T_C = 25°C 1 Watt Max

$V_{BR(DSS)}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amp)	Device	$I_{D(Cont)}$ (Amp) Max
200	0.8	0.4	IRFD220	0.8
	1.2	0.4	IRFD222	0.7
	1.5	0.3	IRFD210	0.6
	2.4	0.3	IRFD212	0.45
150	0.8	0.4	IRFD221	0.8
	1.5	0.3	IRFD211	0.6
	2.4	0.3	IRFD213	0.45
100	0.3	0.6	IRFD120	1.3
	0.4	0.6	IRFD122	1.1
	0.6	0.8	IRFD110	1
	0.6	−0.8	IRFD9120	−1
	0.8	0.8	IRFD112	0.8
	0.8	−0.8	IRFD9122	−0.8
	1.2	−0.3	IRFD9112	−0.6
	1.2	−0.3	IRFD9110	−0.7
	2.4	0.25	IRFD1Z0	0.5
	3.2	0.25	IRFD1Z2	0.4
60	0.3	0.6	IRFD121	1.3
	0.4	0.6	IRFD123	1.1
	0.6	0.8	IRFD111	1
	0.6	−0.8	IRFD9121	−1
	0.8	0.8	IRFD113	0.8
	0.8	−0.8	IRFD9123	−0.8
	2.4	0.25	IRFD1Z1	0.5

Small-Signal MOSFETs (continued)



TO-226AA
(TO-92)

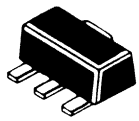
TMOS™

Table 14 — Plastic — TO-226AA Style 22

$V_{(BR)DSS}$	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amp)	Device	$I_{D(Cont)}$ (Amp) Max	P_D @ T_C = 25°C Watts Max
240	6	0.5	VN2406L	0.158	0.4
	10	0.5	VN2410L	0.12	0.4
200	6.4	0.25	BS107A	0.25	0.6
	6.4	0.25	MPF9200	0.4	0.5
	14	0.2	BS107	0.25	0.6
180	140	0.01	MPF481	0.02	0.35
170	6	0.5	VN1706L	0.158	0.4
	10	0.5	VN1710L	0.12	0.4
150	12	0.1	MPF4150†	0.25	0.625
80	80	0.01	MPF480	0.08	0.35
60	5	0.5	2N7000	0.5	0.4
	5	−0.2	BS170P	−0.195	0.4
	5	0.2	BS170	0.195	0.4
	5	0.5	VN0610LL	0.12	0.4
	7.5	0.5	2N7008	1	0.4
	7.5	0.5	VN2222LL	0.099	0.4
30	1.2	1.0	VN0300L	0.4	0.4
	2.5	−1.0	VP0300L	−0.2	0.4

†Depletion Mode

CASE 318-02
SOT-23

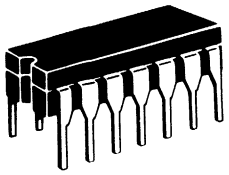


CASE 345-01
SOT-89

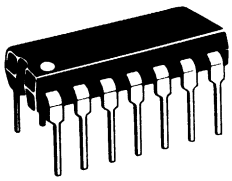
Table 15 — Surface Mount — Case 318-02 Style 10 Case 345-02 Style 5

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amp)	Device	$I_{D(Cont)}$ (Amp) Max	P_D @ T_C = 25°C Watts Max	Package
500	50	0.1	MXF500**	2	0.55	345-02
350	35	0.1	MXF350**	2	0.55	345-02
200	6	0.4	BSS87	0.5	0.55	345-02
100	6	0.1	BSS123	0.17	0.2	318-02
90	2	1	MXF990	2	0.55	345-02
60	1.7	1	MXF960	2	0.55	345-02
	5	0.2	MMBF170	0.5	0.2	318-02
	7.5	0.5	2N7002	0.8	0.2	318-02
35	1.4	1	MXF930	2	0.55	345-02

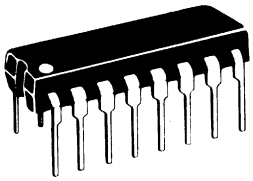
**Introduction Q4/86



CASE 632-02
(TO-16)
14-Pin DIP
Ceramic



Case 646-05
(14-Pin DIP)
Plastic



Case 648-05
(16-Pin DIP)
Plastic

Table 16 — Quad TMOS FETs — Case 632-02, Case 646-05, Case 648-05

$V_{BR(DSS)}$	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amp)	Device	$I_{D(Cont)}$ (Amp) Max	P_D @ T_C = 25°C (Watt) Total Package Max	Package
200	1.4	0.25	MFQ107P	0.25	3	645-05
	6.2	0.2	MPQ200P	0.4	3	645-05
	6.4	0.25	MFQ107AP	0.25	3	645-05
100	0.6	0.8	IRFE110	1	3	648-05
	0.8	−0.8	IRFE9120	1	3	648-05
90	2	1	MFQ990C	2	4	632-02
	2	1	MFQ990P	2	3	646-05
	4	1	MFQ6661P	2	3	646-05
60	0.6	0.8	IRFE9123	0.8	3	648-05
	0.8	0.8	IRFE113	0.8	3	648-05
	1.7	1	MFQ960C	2	4	632-02
	1.7	1	MFQ960P	2	3	646-05
	3	1	MFQ6660C	2	4	632-02
	10	0.5	MFQ1000C	3	4	632-02
35	1.4	1	MFQ930C	2	4	632-02
	1.4	1	MFQ930P	2	3	646-05
	1.8	1	MFQ6659P	2	3	646-05
	2	0.5	MFQ1000P	3	3	646-05

Table 17 — TMOS Product Matrix

I_D (AMP) / $V_{(BR)DSS}$ Volts	0.01–0.49	0.5–0.79	0.8–0.99	1–1.9	2–2.9	3–3.9	4–4.9	5–6	7
1000 950				MTM/MTP 1N100/95		MTM/MTP 3N100/95	MTM/MTH 5N100/95		
900 850					MTM/MTP 2N90/85		MTM/MTP 4N90/85	MTM/MTH 6N90/85	
800 650						MTM/MTP 3N75/80		BUZ84,A	
600 550				MTP 1N60/55	MTM/MTP 2N60/55	MTM/MTP 3N60/55		MTM/MTH/ MTP 6N60/55	
500 450				MTP 1N50/45	MTM/MTP 2N50/45 MTM/MTP 2P50/45 IRF420–23 IRF820–23 MXF500*	MTM/MTP 3N45/50	MTM/MTP 4N50/45 2N6761 2N6762 IRF430–33 IRF830–33		MTM/MTH 7N50/45 IRF842 IRF843 IRF442 IRF443
400 350					MTP 2N40/35 IRF322 IRF323 IRF722 IRF723 MXF350*	MTM/MTP 3N40/45 IRF320 IRF321 IRF720 IRF721	2N6759 MTM/MTP 4N35/40	MTM/MTP 5N40/35 2N6760 IRF330–33 IRF730–33	
250 170	IRFD212 MFE9200 MPF9200 BS107,A VN2406L VN2410L MPQ200P MFQ107P,AP VN1706B VN1710B MPF481	BSS87 IRFD210 IRFD222 VN2406B VN2410B	IRFD220	BS170 BS107	2N6784 MTP 2N20/18 MTP 2N25 IRF610–12	IRFF220 IRFF222 MTM/MTP 3P25 2N6790	IRF222 IRF622 MTP 4N18/20 IRF220 IRF620 MTD4N18 MTD4N20	MTM/MTP 5N20/18 MTM/MTP 5P18/20 MTM/MTP 5P25	MTM/MTP 7N20/18
150 120	IRFD213 MPF4150	IRFD211 IRFD223	IRFD221		IRF611–13	IRFF221 IRFF223 MTP 3N15/12	IRF223,623 MTP 5N12/15 IRF221 IRF621	MTD6N12 MTD6N15	MTM/MTP 7N15/12
100 80	BSS123 IRFD1Z2 MPF480	IRFD120 IRFD9110 IRFD9112 IRFD1Z0	IRFD112 IRFD9122 2N6661	IRFD110 IRFD120 IRFD122 IRFD9120 IRFE110 IRFE9120	2N6661 MFQ/MPF6661 MPF990 MFE990 MFQ990C,P MFX990	2N6782 IRF512 IRFF110 IRFF112	MTP 4N10/08 IRF510	MTP 6N08/10 2N6788 IRFF120 IRFF122	IRF122 IRF522
60 50	2N7008 IRFD123 VN0610LL VN2222LL BS170 BS170P	2N7000 BS1700 MMBF170 MPF910 BS170 IRFD1Z1	IRFD113 IRFD9123 IRFE113 IRFE9123 2N7002	IRFD121 IRFD123 IRFD9121 IRFD111 MFE910 2N6660 2N7008	MPF6660 MFE960 MPF960 MFQ960C,P MXF960 MFQ6660C	IRF513 IRFF111 IRFF113	IRF511 MTD4P05 MTD4P06	IRFF121 IRFF123 MTP 5N06/05 MTM/MTP 5P06/05 MTD5N05 MTD5N06	IRF123 IRF523 MTP 7N05/06 MTM/MTP 7P05/06
40 30	VN0300L VP0300L			VN0300B VN0300P 2N6659	MFE930 MFQ6659P MFQ930C,P MPF930 MXF930 MPF6659	MFQ1000P			

MTM Prefix — TO-204
MTP Prefix — TO-220AB
MTH Prefix — TO-218AC
MTD Prefix — DPAK
*To be introduced.

MFE Prefix — TO-205AD (TO-39)
MPF Prefix — TO-226AA (TO-92)
MFQ Prefix — TO-116
MTE Prefix — Case 353

IRF100 thru 400 Series — TO-204
IRF500 thru 800 Series — TO-220AB
MXF — Case 345-01

IRFD Prefix — Case 370-01
IRFE Prefix — Case 648-05
IRFF Prefix — TO-205AF Type

8	9–10	12–13	14–19	20–24	25–29	30–40	50–75	100–200	I_D (AMP) $V_{(BR)DSS}$ Volts
									1000 950
									900 850
									800 650
MTM/MTH 8N60/55				MTE 20N60/55					600 550
IRF440 IRF441 IRF840 IRF841 MTP8N45 MTP8N50		IRF450 IRF451 MTH13N45 MTH13N50 IRF452 IRF453	MTM/15N 50/45		MTE 25N50/45				500 450
MTM/MTH 8N40/35 IRF742 IRF743 IRF342 IRF343	MTP 10N35/40 IRF740 IRF741 IRF340 IRF341	IRF352 IRF353	MTM/MTH 15N40/35 IRF350 IRF351			MTE 30N40/35			400 350
MTM/MTP 8N20/18 IRF232 IRF632 MTM/MTH 8P18/20 MTM/MTP 8P25	MTM/MTP 10N25 2N6758 IRF230 IRF630	MTM/MTP 12N20/18	IRF240,640 MTM 15N20/18 IRF242,642 MTH 15N20/18		IRF252	IRF250 MTM 40N20/18 MTH 30N20/18	MTE 60N20/18		250 180
IRF233 IRF633 2N6757 MTM/MTP 8N12/15	MTM/MTP 10N15/12 IRF231 IRF631 2N6757		MTM/MTP 15N15/12 IRF241,641 IRF243,643	MTM/MTH 20N15/12	IRF253	IRF251 MTM 45N15/12 MTH 35N15/20	MTE 65N15/12		150 120
MTM/MTP 8N10/08 MTM/MTP 8P10/08 IRF120 IRF520	MTM/MTP 10N10/08 MTP 10N10M	MTM/MTP 12N10/08 12P10/08 IRF132 IRF532	2N6756 IRF130 IRF530 MTH/MTM 15P08/10	MTM/MTP 20N10/08 IRF142 IRF542 MTM/MTH 20P08/10	MTM/MTP 25N10/08 MTH 25N10/08 IRF140 IRF540	IRF150,152 MTH40N 10/08	MTE 75N10/08 MTM 55N10/08		100 80
IRF121 IRF521 MTD3055A	MTM/MTP 10N06/05 MTD10N05A	MTM/MTP 12N06/05 12P06/05 2N6755 IRF133 IRF533 BUZ10	MTM/MTP 15N06/05 IRF131 IRF531 MTP3055A MTP14N05A MTP16N05A MTM/MTP 7P15N05/06L	IRF143 IRF543 MTM/MTP 20P06	MTM/MTP 25N06/05 IRF141 IRF541 MTM/MTH 25P06/05 BUZ11A MTM/MTP 25N05/06L	MTM/MTH 35N06/05 IRF151 IRF153 MTH 40N06/05 BUZ11	MTM 60N06/05	MTE 100N06/05	60 50
									40 30

MOTOROLA SEMICONDUCTOR SALES OFFICES

EUROPE

AUSTRIA
Motorola Ges.m.b.H.
Alserbachstrasse 30
A-1090 Wien
Tel. (0222) 31 65 45

DENMARK
Motorola Semiconductors A/S
Tornerosevej 127
2730 Herlev
Tel. 452 92 00 99

FRANCE
Motorola Semiconducteurs Commerciale S.A.
Main Sales Office
2, rue Auguste-Comte – Bp. 39
92173 Vanves-Cedex
Tel. 4736 01 99

Sales Offices
Chemin de Malacher-Zirst
38240 Meylan (Grenoble)
Tel. (76) 90 22 81

107 Avenue De Crimee
35000 Rennes
Tel. 1699538888

Avenue Général-Eisenhower
31023 Toulouse Cedex
Tel. (61) 41 90 00

FINLAND
Motorola AB
Mannerheimintie 20A
00100 Helsinki
Finland
Tel: 694-8465

WEST GERMANY
Motorola GmbH.
Geschäftsbereich Halbleiter
Main Sales Office
Arabellastrasse 17
8000 München 81
Tel. (089) 92 720

Sales Offices
Hans-Böckler-Strasse 30
3012 Langenhagen
Tel. (0511) 78 99 11

Donaustrasse 43
8500 Nürnberg
Tel. (0911) 643044

Stralsunder-Strasse 1
7032 Sindelfingen
Tel. (0703) 18 30 74 75

Abraham-Lincoln-Strasse 22
6200 Wiesbaden
Tel. (06121) 76 19 21

HOLLAND
Motorola B.V.
Semiconductor Division
Maarssenbroeksedijk 37
3606 AG Maarssen
Tel. (030) 43 96 53

ITALY
Motorola S.p.A.
Divisione Semiconduttori
Main Sales Office
Centro Milanofiori-Strada 2-C2
20090 Assago (Milano)
Tel. (02) 822 01

Sales Office
Via Constantino Maes 68
00162 Roma
Tel. (06) 8322 186

NORWAY
Motorola A/S
Plogveien 1A,
N-0679 Oslo 6
Tel. (02) 198070

SPAIN
Motorola España S.A.
Alberto Alcocer, 46 Dpdo
28016 Madrid
Tel. 457 82 04

SWEDEN
Motorola AB.
Dalvägen 2
S-17136 Solna
Tel. (08) 83 02 00

SWITZERLAND
Motorola (Schweiz) AG
Main Sales Office
Uitikonerstr. 9
8952 Schlieren
Tel. (01) 730 40 74

Sales Office
16, chemin de la Voie-Creuse
P.O. Box 8
1211 Genève 20
Tel. (022) 99 11 11

UNITED KINGDOM
Motorola Ltd.
Main Sales Office
Motorola House
69 Buckingham Street
Aylesbury, Bucks, HP20 2NF
Tel. 0296 395252

Sales Office
Colvilles Road, Kelvin Estate
East Kilbride, Scotland G75 0TG
Tel. (03552) 39101

European Literature Centre
88 Tanners Drive, Blakelands
Milton Keynes MK14 5BP
Tel. (0908) 614614

HEADQUARTERS EUROPEAN OPERATIONS
Motorola Inc.
European Semiconductor Division
16, chemin de la Voie-Creuse
P.O. Box 8
1211 Genève 20
Switzerland
Tel. (022) 99 11 11

EUROPEAN FACTORIES

FRANCE
Motorola Semiconducteurs S.A.
Avenue Général-Eisenhower
31023 Toulouse CEDEX
Tel. (61) 41 90 00

GERMANY
Motorola GmbH
Münchner Strasse 18
8043 Unterföhring
Tel. (089) 92 481

UNITED KINGDOM
Motorola Limited
Colvilles Road, Kelvin Estate
East Kilbride, Scotland G75 0TG
Tel. (03552) 39101

YOUR LOCAL DISTRIBUTOR IS:

MOTOROLA ***Semiconducteurs S.A.***
AVENUE GÉNÉRAL EISENHOWER, 31023 TOULOUSE CEDEX, FRANCE

Printed in Great Britain - Watkiss Studios - 7/87 - 50